P.S. Software House
Marketing And Research Co.
P.O. Box 966
Mishawaka, IN 46544
(219) 255-3408

Dear PET owner;

Thank you for your order. We at PET-SHACK take great Pride in our Products and hope you are completely satisfied. In fact we Guarantee your satisfaction or we will Sadly but Promptly refund your money.

Take a look at the enclosed list of our Fine Products and see if there is anything else we can serve you with.

We solicit your suggestions on improvements and New products.

We hope to be able to serve you again.

Sincerely,

Larry R. Shallenberger

Larry R. Shallenberger President

**P.S. Software House**
**Marketing And Research Co.**
**P.O. Box 966**
**Mishawaka, IN 46544**

ERRATA: Corrections and Differences for the PET schematics.

On the CPU board layout, three misprints were found.

| | | |
|---|---|---|
| G1 | should be | SN74154 |
| E4 | should be | 74LS154 |
| B7 | should be | 6520 |

---

It was brought to my attention by one of my customers that on his PET the ROM's are 24 pin #901447-01 to 07 with the 01's being replaced by 09's to eliminate the problem of losing the curser. With this series, there is no need for additional chips for decoding or inverting signals. I do not have the pin-outs for this series as of yet. After I have compiled a substantial list of changes, I will send this list to all who requist it.

# PETSHACK Software House

*MARKETING AND RESEARCH COMPANY*

P. O. Box 966 Mishawaka, Indiana 46544

(219) 255 3408


Re. ROM & RAM chips:

The ROM chips and the RAM chips used in your PET may not be the same as used in the authors PET. According to the best information I have been able to get at this time, Commodore is using two different chips of each. For the RAM's they are using either the 6550 or the 2114(6114) and for the ROM's they are either using the 6540 or the 2316(6316). Even though the pin-outs are different, the function is identical so the actual wireing should be identical, with the exception of the Chip Select lines.

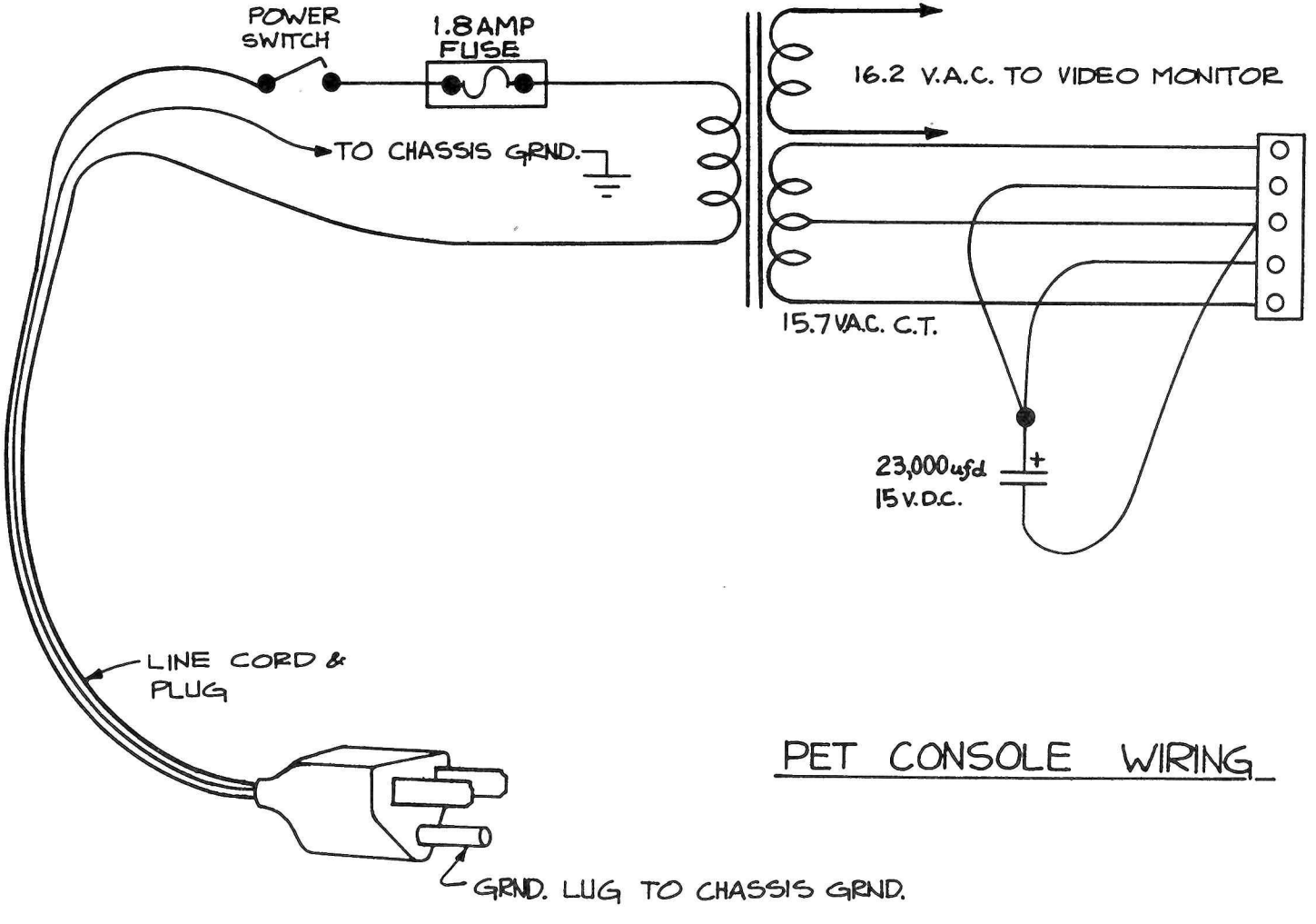
Where the 2316 is used in place of the 6540, inverters have to be added in line to two of the Chip Select lines (CS1,CS2, or CS3). The implementation of the 2114 in place of the 6550 is a bit more difficult in that it has only one Chip Select line. A 74LS139 has to be added to decode the Address lines to replace the missing Chip Select lines. A partial schematic is included to show the changes.

Enclosed in this package are the specification and Pin-Out sheets of all five chips mentioned.

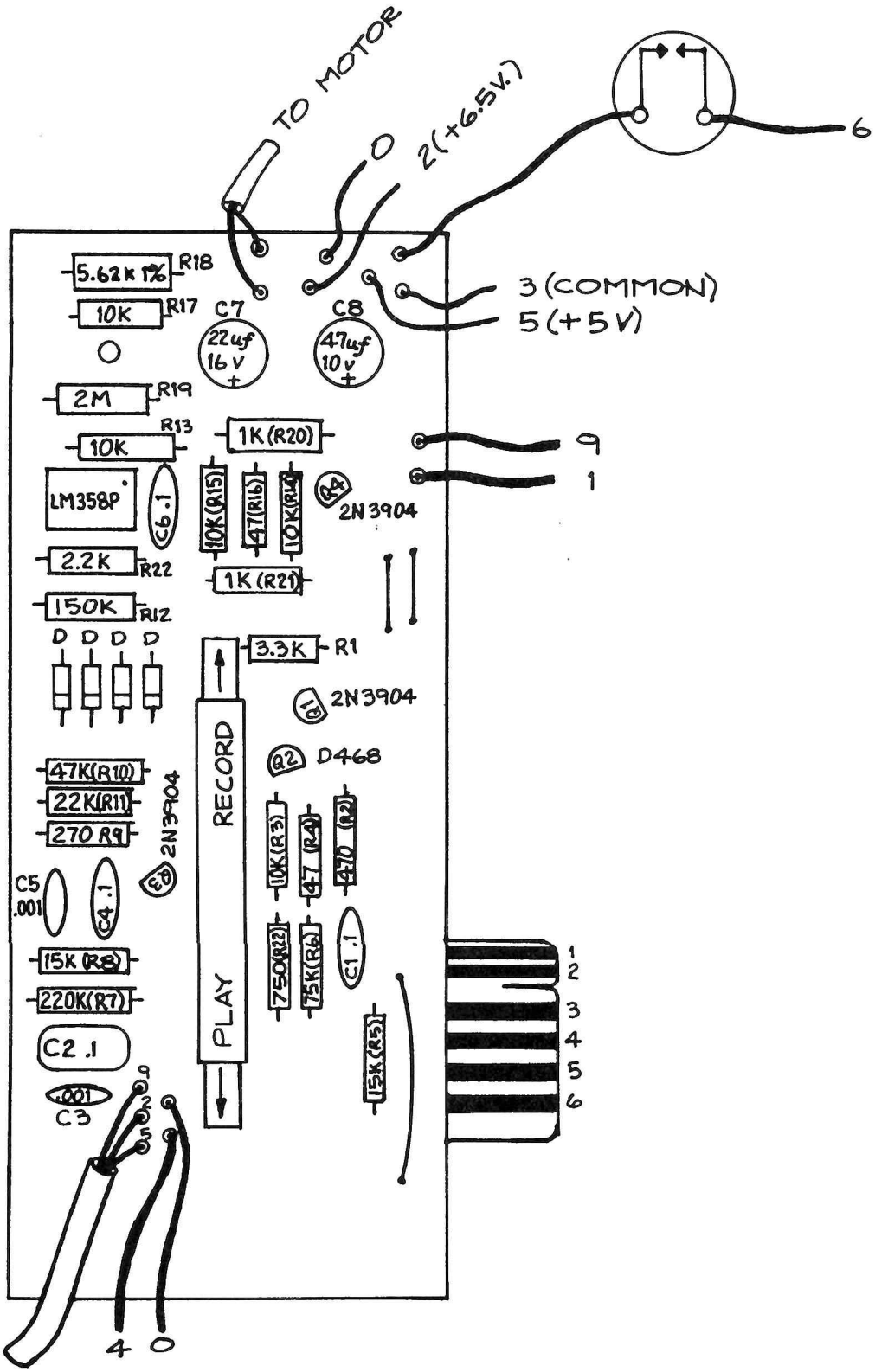
If you find any other differences, I would appreciate it if you would let me know so that I can update future schematics.

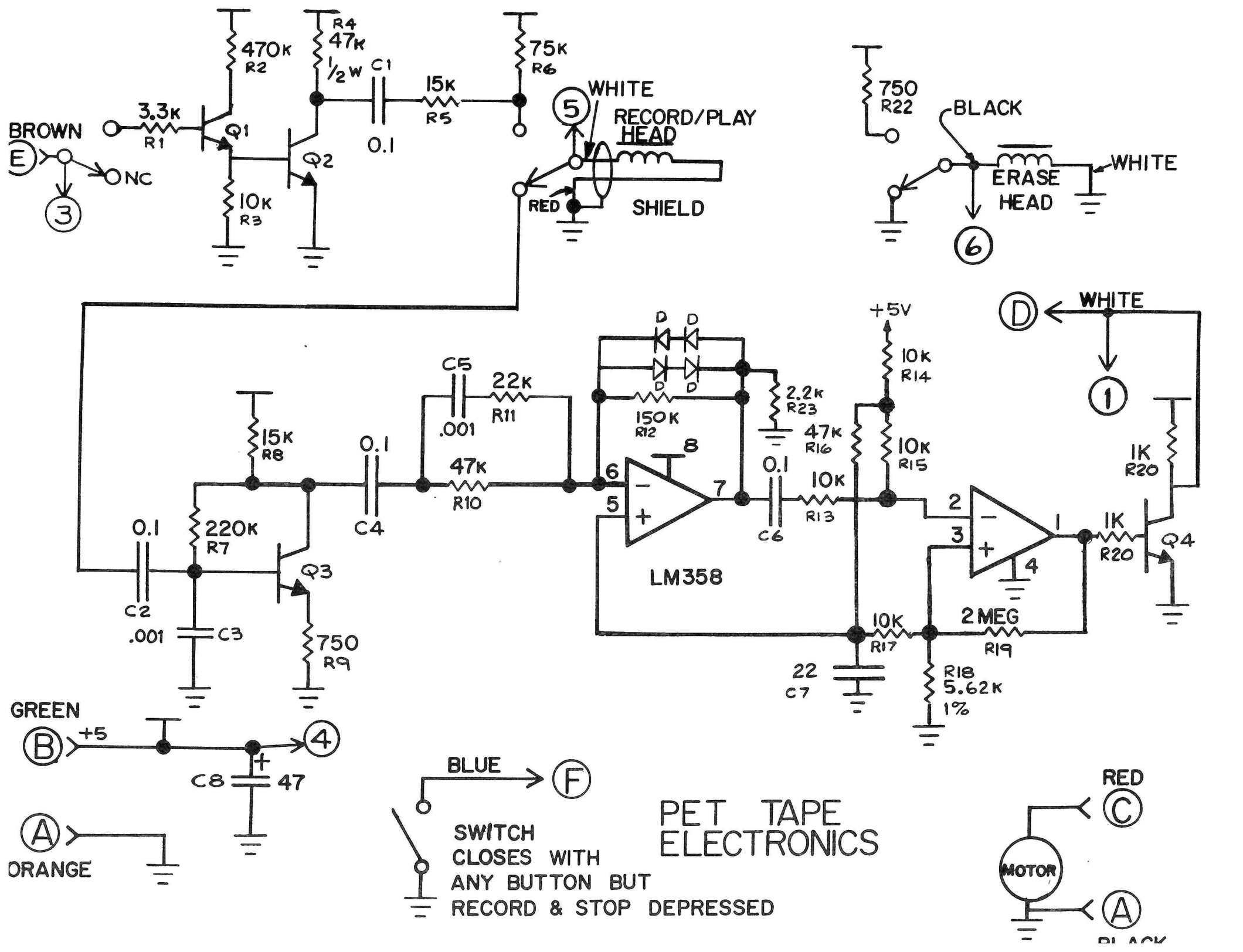
Larry R. Shallenberger

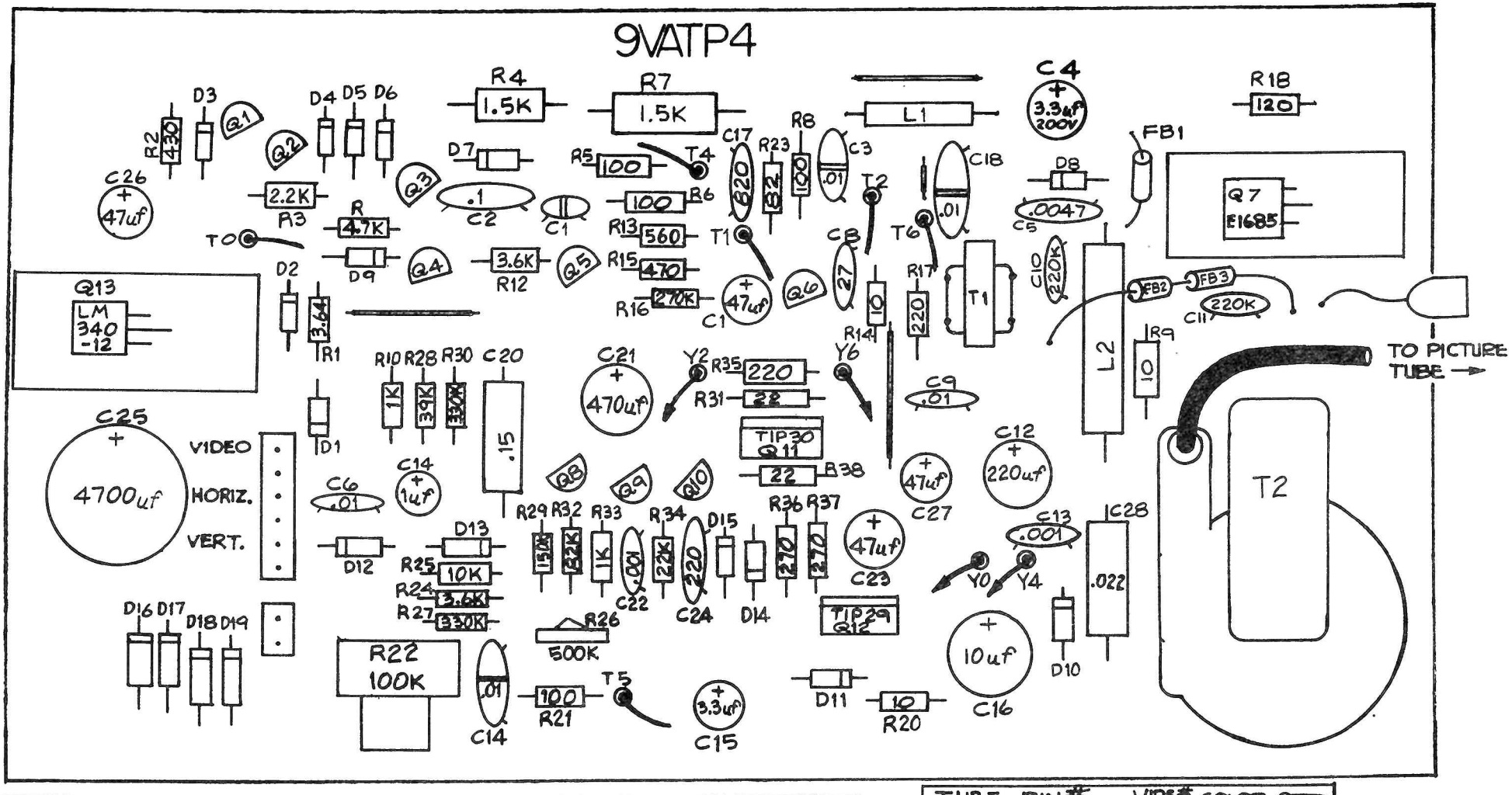
LARRY R. SHALLENBERGER President




PET CONSOLE WIRING


TO MOTOR
2(+6.5V.)
6
3(COMMON)
5(+5V)
5.62K 1% R18
10K R17
C7 22uf 16V
C8 47uf 10V
2M R19
10K R13
1K (R20)
9
1
LM358P
C6 .1
10K(R15)
47(R16)
10K(R14)
Q4 2N3904
2.2K R22
1K (R21)
150K R12
D D D D
3.3K R1
Q1 2N3904
Q2 D468
47K(R10)
22K(R11)
270 R9
Q3 2N3904
C5 .001
C4 .1
15K (R8)
220K(R7)
C2 .1
.001 C3
RECORD
PLAY
10K(R3)
47 (R4)
470 (R2)
750(R22)
75K(R6)
C1 .1
15K(R5)
1
2
3
4
5
6
4
0


470K
R2
R4
47K
1/2W
C1
15K
R5
75K
R6
3.3K
R1
Q1
Q2
0.1
10K
R3
BROWN
E
NC
3
5
WHITE
RECORD/PLAY
HEAD
RED
SHIELD
750
R22
BLACK
ERASE
HEAD
WHITE
6
D
WHITE
1
+5V
10K
R14
2.2K
R23
150K
R12
C5
22K
R11
.001
15K
R8
0.1
C4
47K
R10
47K
R16
10K
R15
0.1
C6
10K
R13
8
6
5
7
LM358
2
3
1
4
1K
R20
Q4
0.1
C2
.001
220K
R7
Q3
C3
750
R9
10K
R17
2 MEG
R19
22
C7
R18
5.62K
1%
GREEN
B
+5
4
C8
47
A
ORANGE
BLUE
F
SWITCH
CLOSES WITH
ANY BUTTON BUT
RECORD & STOP DEPRESSED
PET TAPE
ELECTRONICS
RED
C
MOTOR
A
BLACK




Y2 & Y6 TO VERTICAL COIL ON DEFLECTION YOKE
Y4 & YO TO HORIZ. COIL ON DEFLECTION YOKE

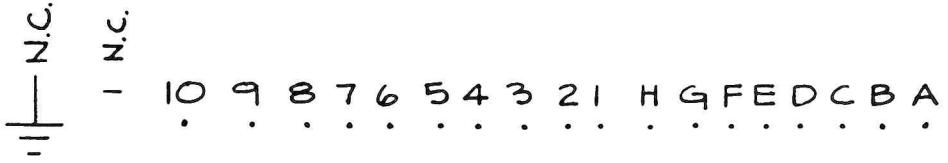
NOTE: THIS SYMBOL ⊙— INDICATES A WIRE LEAD ENDING @ DEFLECTION YOKE (MARKED "Y") OR CRT (TUBE; MARKED "T").

| TUBE PIN # | WIRE # COLOR |
|---|---|
| 1 | T5-GREEN |
| 2 | T4-YELLOW |
| 3 | T1-BROWN |
| 4 | T0-BLACK |
| 5 | N.C. |
| 6 | T2-RED |
| 7 | T6-BLUE |

# VIDEO MONITOR

NOT USED:

2F
4F
6F
8F
10F

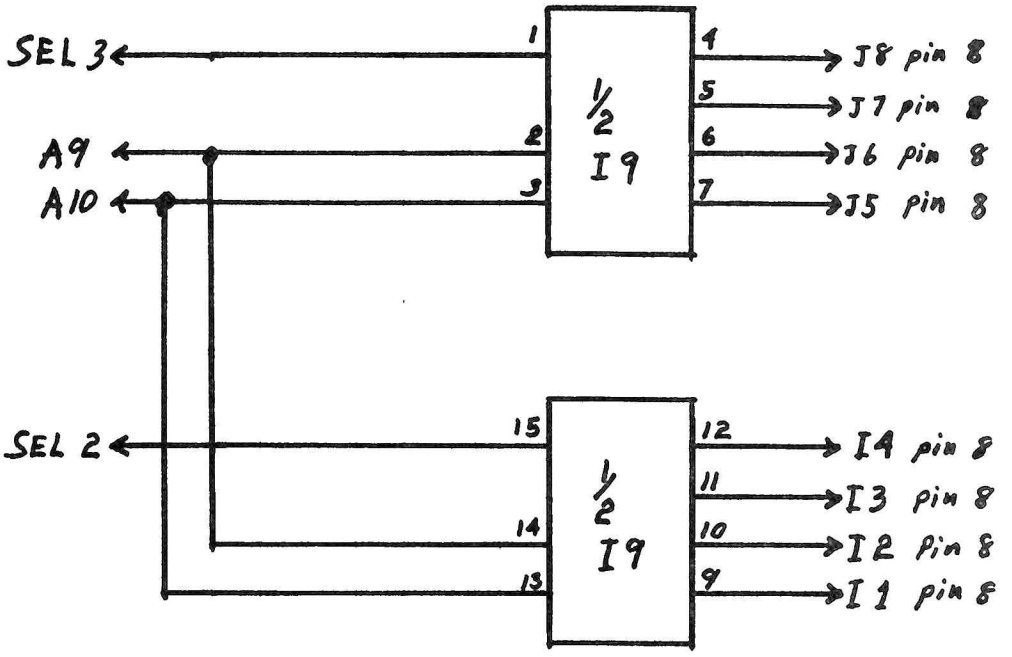


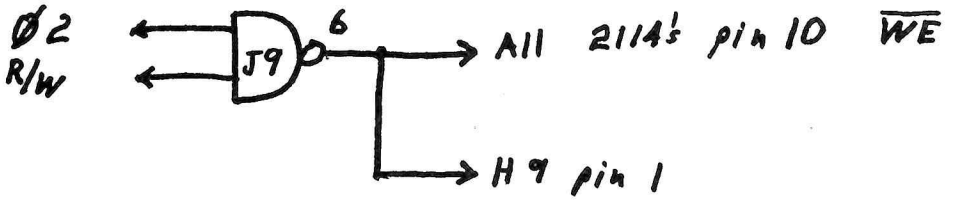

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 A | 2 A | 1 B | 2 B | 1 C | 2 C | 1 D | 2 D | 1 E | 2 E | 1 F |
| 3 A | 4 A | 3 B | 4 B | 3 C | 4 C | 3 D | 4 D | 3 E | 4 E | 3 F |
| 5 A | 6 A | 5 B | 6 B | 5 C | 6 C | 5 D | 6 D | 5 E | 6 E | 5 F |
| 7 A | 8 A | 7 B | 8 B | 7 C | 8 C | 7 D | 8 D | 7 E | 8 E | 7 F |
| 9 A | 10 A | 9 B | 10 B | 9 C | 10 C | 9 D | 10 D | 9 E | 10 E | 9 F |

| | | | |
|---|---|---|---|
| 1 G | 2 G | 1 H | 2 H |
| 3 G | 4 G | 3 H | 4 H |
| 5 G | 6 G | 5 H | 6 H |
| 7 G | 8 G | 7 H | 8 H |
| 9 G | 10 G | 9 H | 10 H |

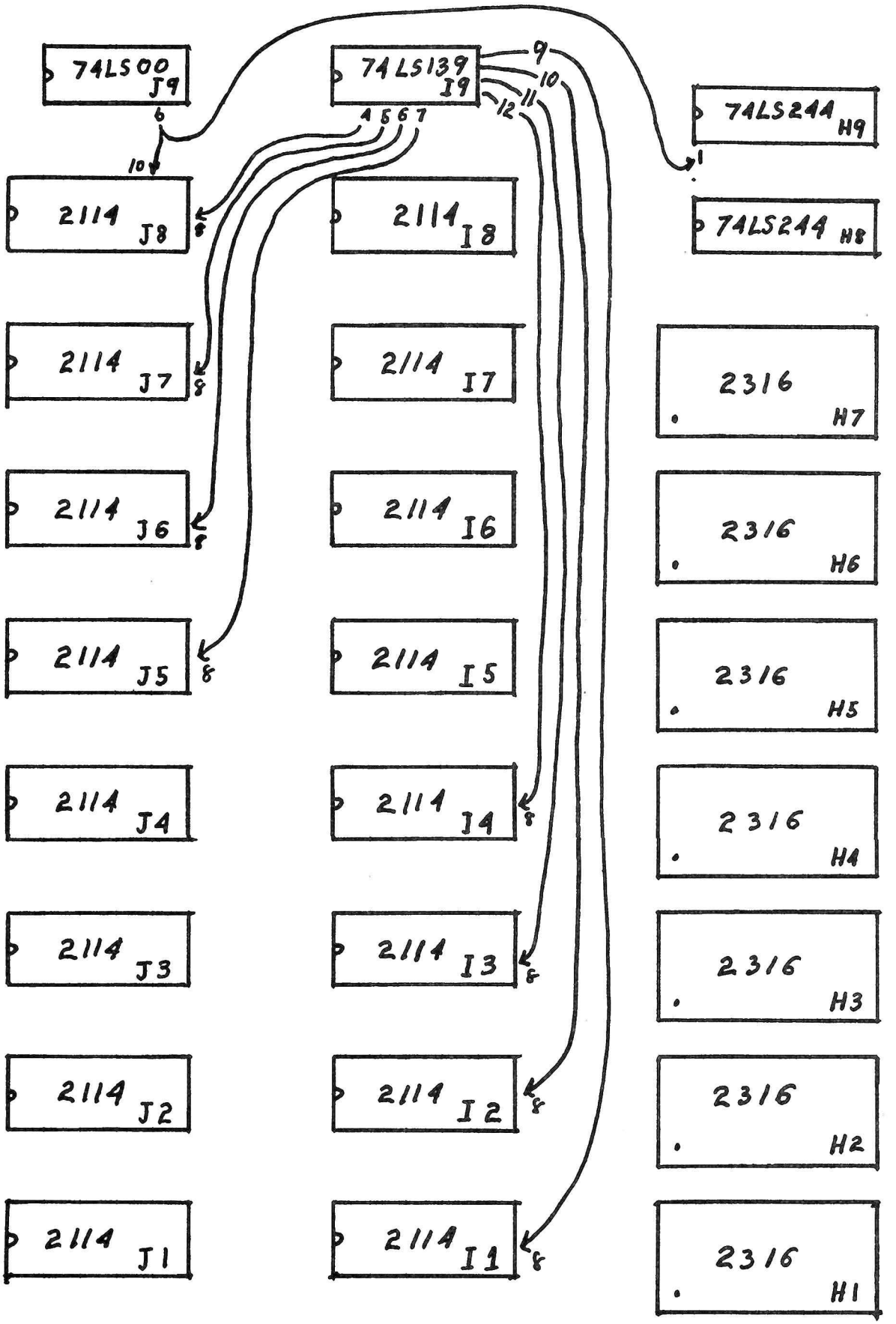
NOTE: EACH NUMBER AND LETTER COMBINATION IN THE SQUARES ABOVE (KEY BOARD KEYS) REFERS TO THE CORRESPONDING NUMBER AND LETTER ON THE CONNECTOR J-5 (SEE PARTS LAYOUT).

PET KEYBOARD




Temp Drawing
L.S.


74LS00 J9
74LS139 I9
74LS244 H9
74LS244 H8
2114 J8
2114 I8
2114 J7
2114 I7
2316 H7
2114 J6
2114 I6
2316 H6
2114 J5
2114 I5
2316 H5
2114 J4
2114 I4
2316 H4
2114 J3
2114 I3
2316 H3
2114 J2
2114 I2
2316 H2
2114 J1
2114 I1
2316 H1
Temp Drawing

# 6550

RANDOM ACCESS MEMORY

(1024 X 4)

The 6550 is a high performance, low power, 4K bit, static, read/write random access memory organized as 1024 words by 4 bits per word. It operates on a single 5V power supply and requires minimum buffering and CS decoding.

All interface signal levels are identical to TTL specification, providing high noise immunity and simplified system design. All inputs are purely capacitive MOS loads with no DC current requirements. The output will drive two standard TTL loads and 100 pf.

The 6550 cycle operation is controlled by the $\emptyset_2$ Clock. Addresses are presented to the address pin when $\emptyset_2$ Clock is low and are latched on chip to the rising edge of the $\emptyset_2$ Clock. The Chip Select and Read/Write signals are static and can be presented to the memory at any time. Data In and Data Out signals share common I/O pins and are unable to receive or transmit data when $\emptyset_2$ Clock is high.

The 6550 outputs are in the high impedance state whenever the memory is de-selected, $\emptyset_2$ Clock is low or Read/Write is low.

## FEATURES

- 1K × 4 Organization
- Single 5V Power Supply
- Full TTL Compatibility
- Four CS Inputs
- Fully Static Data Storage - No Refreshing
- High Speed - Access Times Down to 200 ns
- Low Operating Power - 450 mW Typical
- Single Phase TTL Level Clock
- High Output Drive - Two Standard TTL Load and 100 pf

## PIN CONNECTIONS

| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | $A_0$ | 8 | $A_6$ | 15 | $DB_2$ |
| 2 | $A_1$ | 9 | $A_7$ | 16 | $DB_3$ |
| 3 | $A_2$ | 10 | $A_8$ | 17 | $V_{DD}$ |
| 4 | $A_3$ | 11 | $A_9$ | 18 | $\overline{CS_4}$ |
| 5 | $A_4$ | 12 | R/W | 19 | $\overline{CS_3}$ |
| 6 | $A_5$ | 13 | $DB_0$ | 20 | $CS_2$ |
| 7 | $\emptyset_2$ | 14 | $DB_1$ | 21 | $CS_1$ |
| | | | | 22 | $V_{SS}$ |

MOS TECHNOLOGY, INC.
VALLEY FORGE CORPORATE CENTER (215) 666-7950
950 RITTENHOUSE ROAD, NORRISTOWN, PA. 19401

PRELIMINARY

DATA

SHEET

JULY 1977

# 6540/6541

## READ ONLY MEMORIES

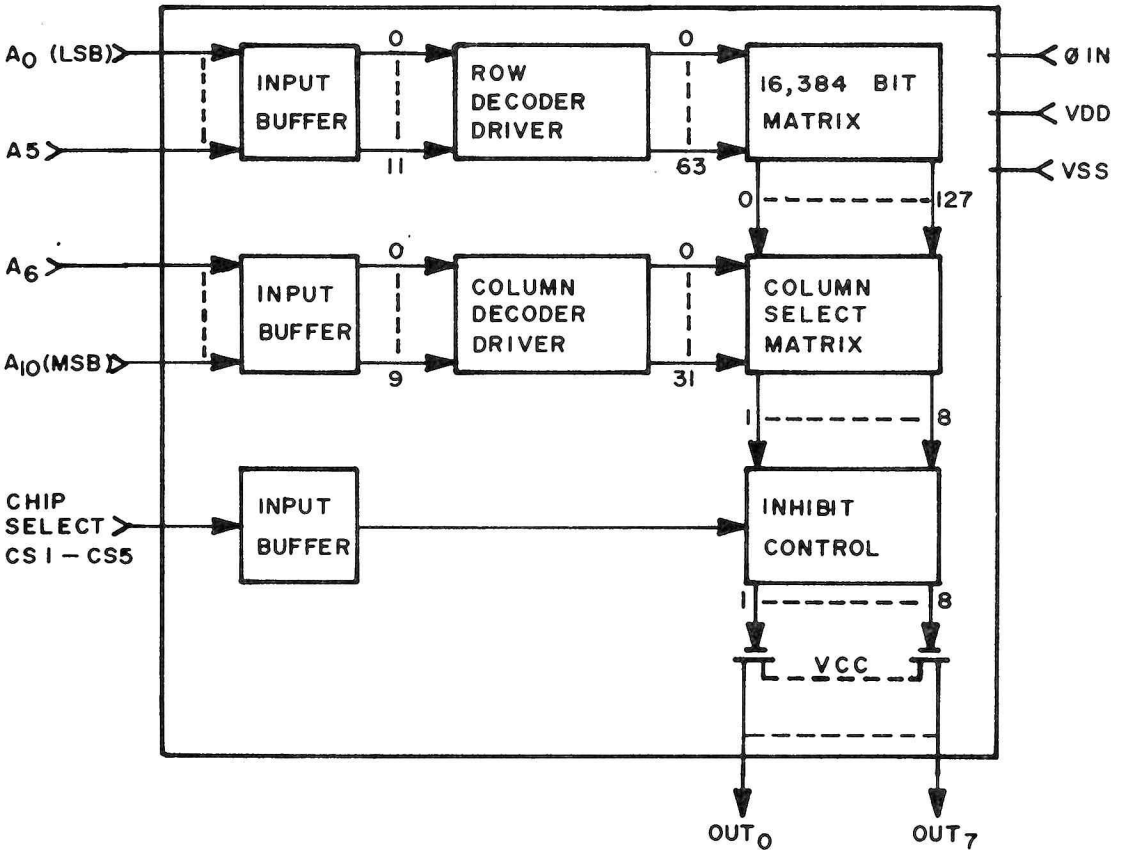
The 6540 and 6541 16K Read Only Memories are monolithic N-channel metal-gate arrays manufactured with a low-threshold process and utilizing both enhancement and depletion mode MOS transistors.

Three-state outputs provide bus-compatibility with microprocessor-based memory systems. The ROM's are organized as 2048 words of 8 bits each.

Mask options provide user specification of chip select equations, allowing addressing anywhere within a 65K memory space without external decode circuitry (6540).

## FEATURES

- Interface with TTL, DTL or MOS
- Single +5V supply
- High speed operation (300 ns access)
- Three-state outputs
- Complete address control
- No external components required
- No system slow-down
- Five chip selects (6540)
- Two chip selects (6541)

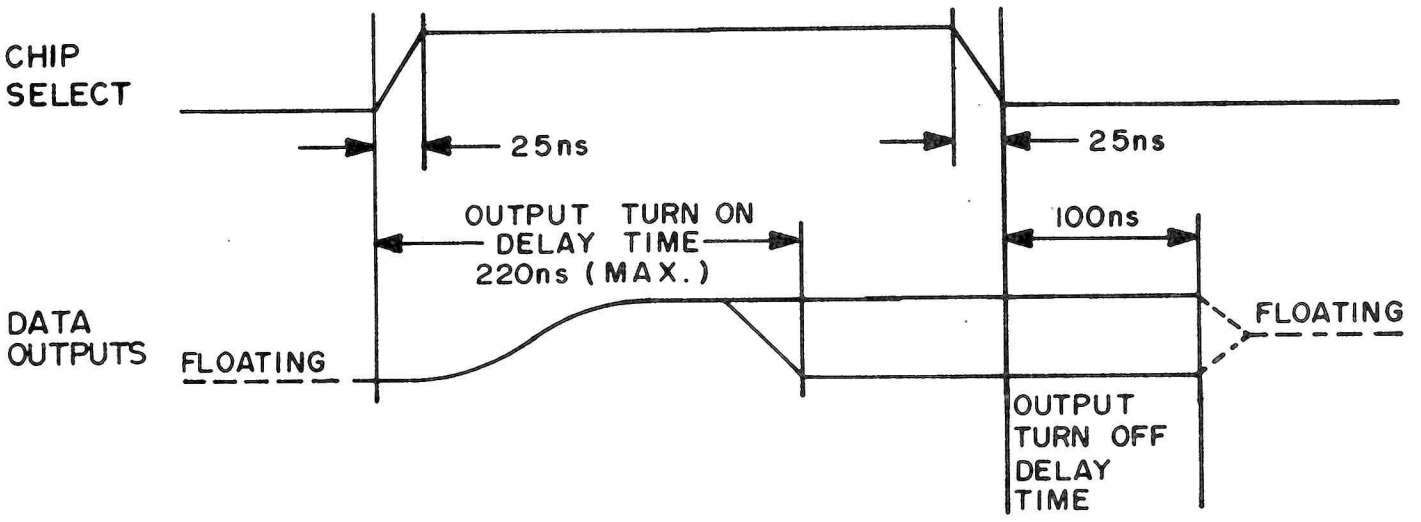


MAXIMUM RATINGS

| RATING | SYMBOL | VOLTAGE | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | V |
| Input/Output Voltage | $V_{IN}$ | -0.3 to +7.0 | V |
| Operating Temperature | $T_{OP}$ | 0 to 70 | °C |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

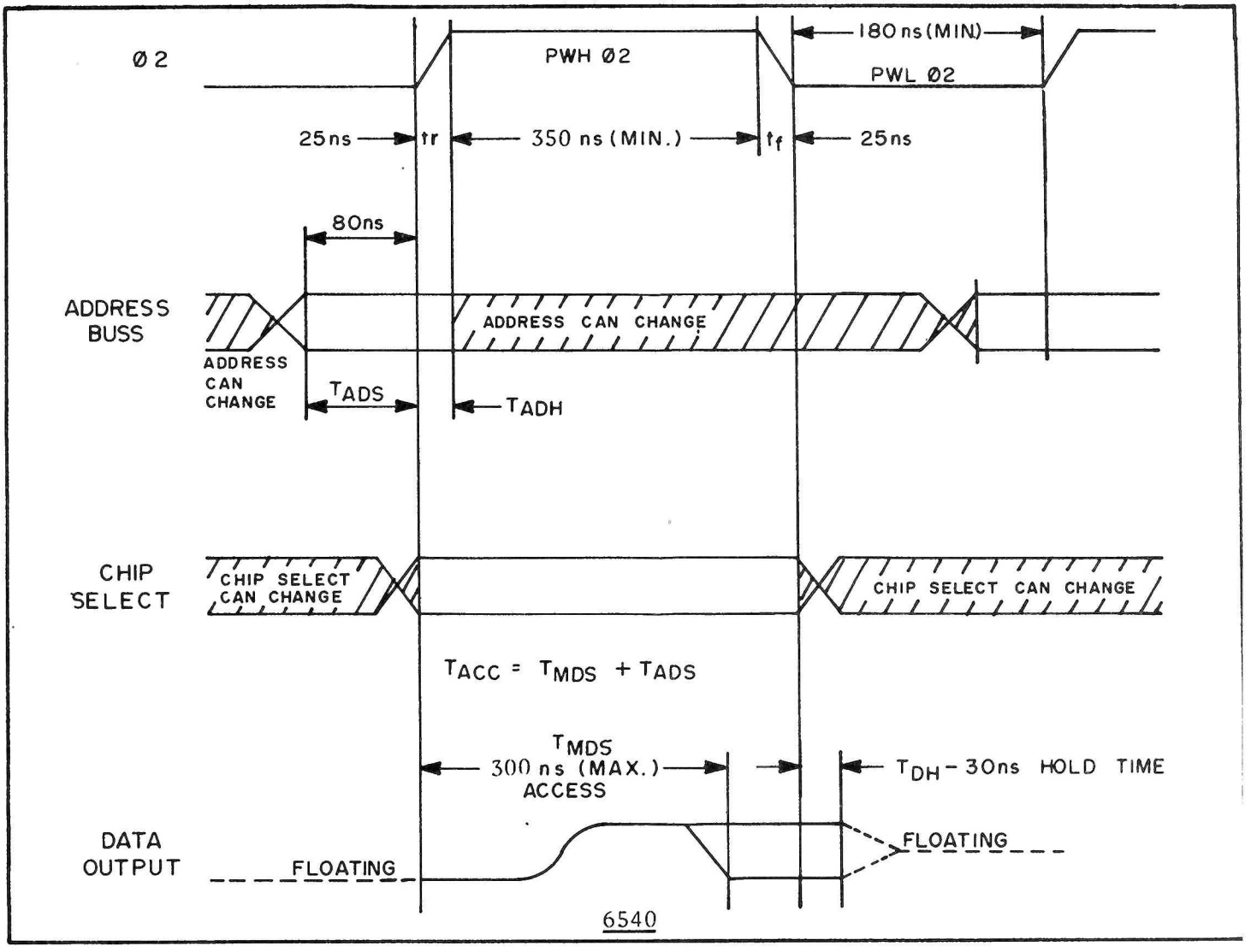
ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0 V ± 5% $V_{SS}$ = 0 V; $T_A$ = 25°C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | Vss+2.0 | - | $V_{CC}$ | V |
| Input Low Voltage | $V_{IN}$ | Vss-.3 | - | Vss+.8 | V |
| Input Leakage Current ($A_0$-$A_{10}$, $C_{S1}$, $C_{S2}$, $\phi_2$) | $I_{IN}$ | | 1.0 | 2.5 | µA |
| Leakage Current for High Impedance (Three State) Outputs: $V_{IN}$ = 0.4 V to 2.4 V | $I_{TSI}$ | | 1.0 | 10.0 | µA |
| Output High Voltage: $V_{CC}$ = Min $I_{LOAD} \leq$ -100µA | $V_{OH}$ | Vss+2.4 | | | V |
| Output Low Voltage $V_{CC}$ = Min $I_{LOAD} \leq$ 1.6 mA | $V_{OL}$ | | | Vss+.4 | V |
| Output Low Current (sinking) $V_{OL} \leq$ .4 V | $I_{OL}$ | 1.6 | | | mA |
| Supply Current Icc | | | 110 | 150 | mA |

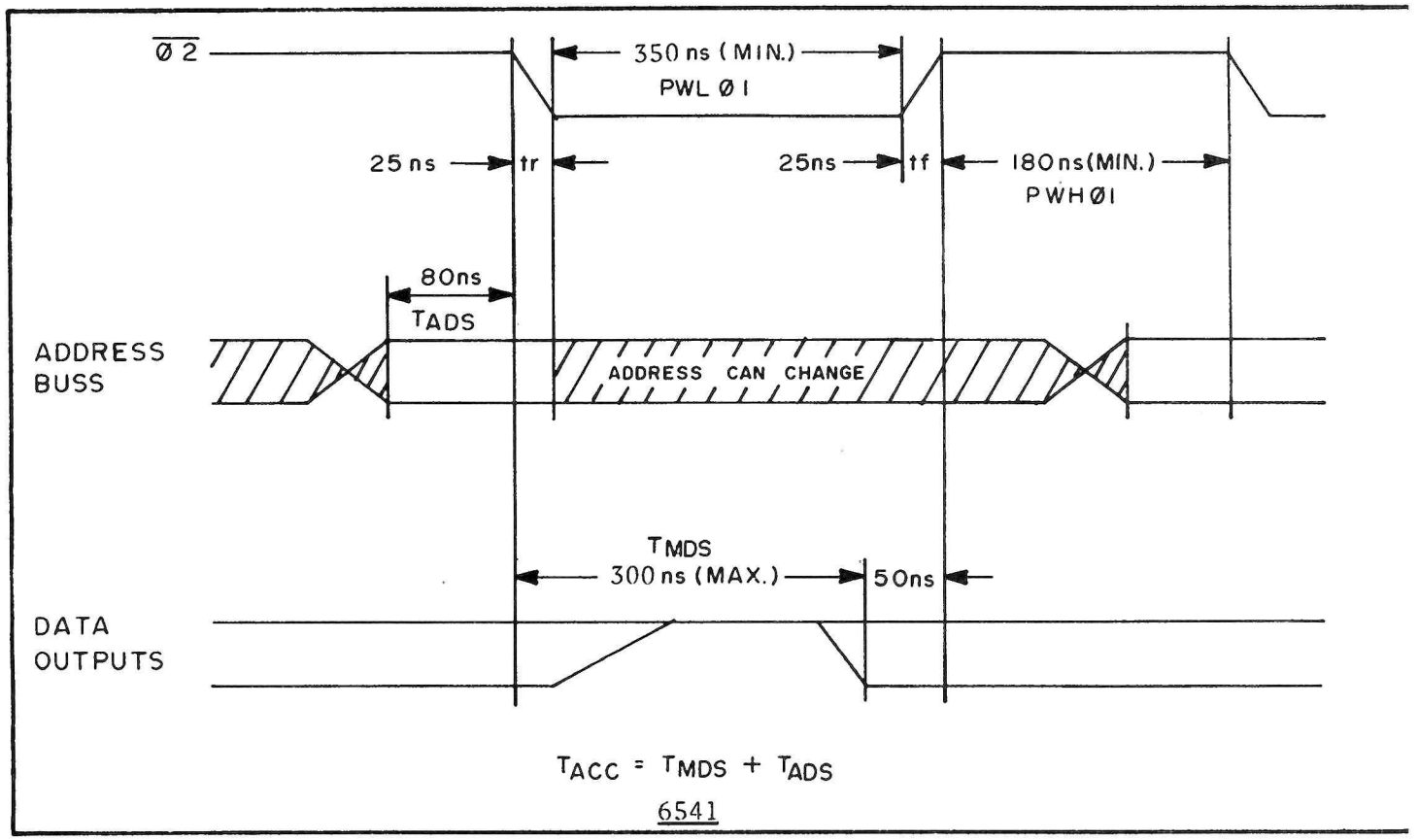



PIN CONNECTIONS

| PIN | 6540 | 6541 | PIN | 6540 | 6541 |
|---|---|---|---|---|---|
| 1 | $V_{ss}$ | GND | 15 | $A_6$ | $A_{10}$ |
| 2 | $CS_5$ | $A_0$ | 16 | $\emptyset_2$ | $DB_7$ |
| 3 | $CS_4$ | $A_3$ | 17 | $CS_1$ | $DB_6$ |
| 4 | $CS_3$ | $A_4$ | 18 | $AI_0$ | $DB_5$ |
| 5 | $A_0$ | $A_3$ | 19 | $DB_7$ | $DB_4$ |
| 6 | $A_1$ | $A_4$ | 20 | $DB_6$ | $DB_3$ |
| 7 | $A_2$ | $A_5$ | 21 | $DB_5$ | $DB_2$ |
| 8 | $A_3$ | $A_9$ | 22 | $DB_4$ | $DB_1$ |
| 9 | $A_4$ | $V_{cc}$ | 23 | $DB_3$ | $DB_0$ |
| 10 | $A_5$ | $A_8$ | 24 | $DB_2$ | $GS_2$ |
| 11 | $A_9$ | $A_7$ | 25 | $DB_1$ | |
| 12 | $V_{cc}$ | $A_6$ | 26 | $DB_0$ | |
| 13 | $A_8$ | $\overline{\emptyset_2}$ | 27 | $CS_2$ | |
| 14 | $A_7$ | $CS_1$ | 28 | N.C. | |


Ø2
PWH Ø2
180 ns (MIN)
PWL Ø2
25ns
tr
350 ns (MIN.)
tf
25ns
80ns
ADDRESS BUSS
ADDRESS CAN CHANGE
ADDRESS CAN CHANGE
TADS
TADH
CHIP SELECT
CHIP SELECT CAN CHANGE
CHIP SELECT CAN CHANGE
TACC = TMDS + TADS
TMDS
300 ns (MAX.)
ACCESS
TDH - 30ns HOLD TIME
DATA OUTPUT
FLOATING
FLOATING

6540


Ø2
350 ns (MIN.)
PWL Ø1
25 ns
tr
25ns
tf
180ns(MIN.)
PWHØ1
80ns
TADS
ADDRESS BUSS
ADDRESS CAN CHANGE
TMDS
300 ns (MAX.)
50ns
DATA OUTPUTS
TACC = TMDS + TADS

6541

# 1024x4 Static Random Access Memory

# SY2114

## MEMORY PRODUCTS

Synertek®



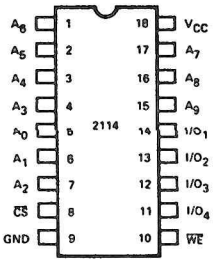
- 300 ns Maximum Access
- Low Operating Power Dissipation 0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 2 TTL loads.

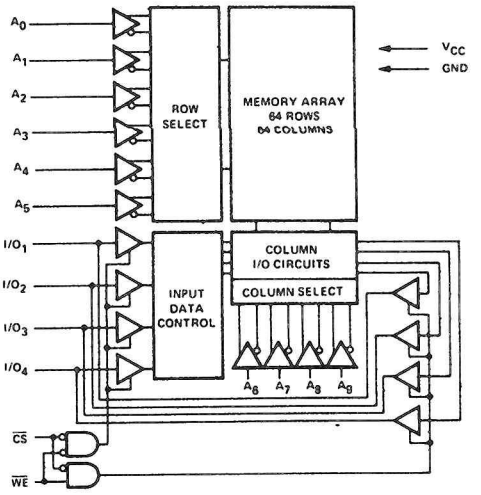
The SY2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.

### PIN CONFIGURATION




### BLOCK DIAGRAM




### ORDERING INFORMATION

| Order Number | Package Type | Access Time | Supply Current (Max) | Temperature Range |
|---|---|---|---|---|
| SYC2114 | Ceramic | 450nsec | 100mamp | 0°C to 70°C |
| SYP2114 | Molded | 450nsec | 100mamp | 0°C to 70°C |
| SYC2114-3 | Ceramic | 300nsec | 100mamp | 0°C to 70°C |
| SYP2114-3 | Molded | 300nsec | 100mamp | 0°C to 70°C |
| SYC2114L | Ceramic | 450nsec | 70mamp | 0°C to 70°C |
| SYP2114L | Molded | 450nsec | 70mamp | 0°C to 70°C |
| SYC2114L-3 | Ceramic | 300nsec | 70mamp | 0°C to 70°C |
| SYP2114L-3 | Molded | 300nsec | 70mamp | 0°C to 70°C |

Synertek® • P.O. Box 552 • Santa Clara, CA 95052 • Telephone (408) 984-8900 • TWX: 910-338-0135

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Temperature Under Bias | -10°C to 80°C |
| Storage Temperature | -65°C to 150°C |
| Voltage on Any Pin with Respect to Ground | -0.5V to +7V |
| Power Dissipation | 1.0W |

## COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## D.C. CHARACTERISTICS $T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±5% (Unless Otherwise Specified)

| Symbol | Parameter | 2114-3, 2114 Min | 2114-3, 2114 Max | 2114L, 2114L-3 Min | 2114L, 2114L-3 Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current (All input pins) | | 10 | | 10 | µA | $V_{IN}$ = 0 to 5.25V |
| $I_{LO}$ | I/O Leakage Current | | 10 | | 10 | µA | $\overline{CS}$ = 2.0V, $V_{I/O}$ = 0.4V to $V_{CC}$ |
| $I_{CC1}$ | Power Supply Current | | 95 | | 65 | mA | $V_{CC}$ = 5.25V, $I_{I/O}$ = 0 mA, $T_A$ = 25°C |
| $I_{CC2}$ | Power Supply Current | | 100 | | 70 | mA | $V_{CC}$ = 5.25V, $I_{I/O}$ = 0 mA, $T_A$ = 0°C |
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.8 | -0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | $I_{OH}$ = -1.0 mA |

## CAPACITANCE $T_A$ = 25°C, f = 1.0 MHz

| Symbol | Test | Typ | Max | Units |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance | | 5 | pF |
| $C_{IN}$ | Input Capacitance | | 5 | pF |

NOTE: This parameter is periodically sampled and not 100% tested.

## A.C. CHARACTERISTICS $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5% (Unless Otherwise Specified)

| SYMBOL | PARAMETER | 2114-3,2114L-3 MIN | 2114-3,2114L-3 MAX | 2114, 2114L MIN | 2114, 2114L MAX | UNIT |
|---|---|---|---|---|---|---|
| READ CYCLE | | | | | | |
| $t_{RC}$ | Read Cycle Time | 300 | | 450 | | nsec |
| $t_A$ | Access Time | | 300 | | 450 | nsec |
| $t_{CO}$ | Chip Select to Output Valid | | 100 | | 120 | nsec |
| $t_{CX}$ | Chip Select to Output Enabled | 20 | | 20 | | nsec |
| $t_{OTD}$ | Chip Deselect to Output Off | 0 | 80 | 0 | 100 | nsec |
| $t_{OHA}$ | Output Hold From Address Change | 50 | | 50 | | nsec |
| WRITE CYCLE | | | | | | |
| $t_{WC}$ | Write Cycle Time | 300 | | 450 | | nsec |
| $t_{AW}$ | Address to Write Setup Time | 0 | | 0 | | nsec |
| $t_W$ | Write Pulse Width | 150 | | 200 | | nsec |
| $t_{WR}$ | Write Release Time | 0 | | 0 | | nsec |
| $t_{OTW}$ | Write to Output Off | 0 | 80 | 0 | 100 | nsec |
| $t_{DW}$ | Data to Write Overlap | 150 | | 200 | | nsec |
| $t_{DH}$ | Data Hold | 0 | | 0 | | nsec |

### A.C. Test Conditions

Input Pulse Levels . . . . . 0.8V to 2.0V
Input Rise and Fall Time . . . . . 10 n sec
Timing Measurement Levels: Input . . . . . 1.5V
Output . . . . . 0.8 and 2.0V
Output Load . . . . . 1TTL Gate and 100pF

# 2048x8 Static Read Only Memory

# SY2316A
# SY2316B

Synertek®

MEMORY PRODUCTS

- 2048x8 Bit Organization
- Single +5 Volt Supply
- Metal Mask Programming
- Two Week Prototype Turnaround
- Access Time–550ns /450ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316A – Replacement for Intel 2316A
- SY2316B – Pin Compatible with 2708 EPROM
  – Replacement for Two 2708s

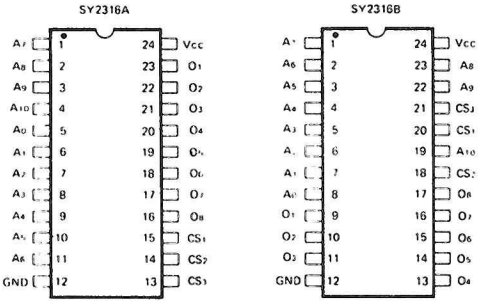
The SY2316A and SY2316B high performance read only memories are organized 2048 words by 8 bits with access times of less than 550 ns and 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The SY2316A/B operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

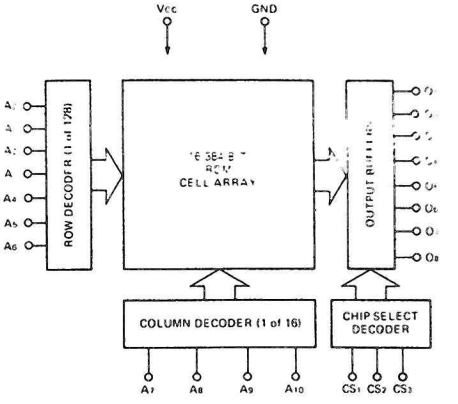
Designed to replace two 2708 8K EPROMs, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

ROMs

## PIN CONFIGURATION




## BLOCK DIAGRAM




## ORDERING INFORMATION

| Order Number | Package Type | Access Time | Temperature Range |
|---|---|---|---|
| SYC2316A | Ceramic | 550ns | 0°C to +70°C |
| SYP2316A | Plastic | 550ns | 0°C to +70°C |
| SYC2316B | Ceramic | 450ns | 0°C to +70°C |
| SYP2316B | Plastic | 450ns | 0°C to +70°C |

A custom number will be assigned by Synertek.

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B-10K-7/76

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Ambient Operating Temperature | 0° to +70°C |
| Storage Temperature | −65°C to +150°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| Applied Output Voltage | −0.5V to +7.0V |
| Applied Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

## COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. CHARACTERISTICS

$T_A$ = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.4 | Vcc | Volts | Vcc = 4.75V, $I_{OH}$ = −200 μA |
| $V_{OL}$ | Output LOW Voltage | | 0.4 | Volts | Vcc = 4.75V, $I_{OL}$ = 2.1 mA |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | Vcc | Volts | |
| $V_{IL}$ | Input LOW Voltage | −0.5 | 0.8 | Volts | See Note 1 |
| $I_{LI}$ | Input Load Current | | 10 | uA | Vcc = 5.25V, 0V ≤ $V_{in}$ ≤ 5.25V |
| $I_{LO}$ | Output Leakage Current | | 10 | uA | Chip Deselected<br>$V_{out}$ = +0.4V to Vcc |
| Icc | Power Supply Current | | 98 | mA | Output Unloaded<br>Vcc = 5.25V, $V_{in}$ = Vcc |

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

## A.C. CHARACTERISTICS

$T_A$ = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

| Symbol | Parameter | SY2316B | | SY2316A | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{ACC}$ | Address Access Time | | 450 | | 550 | ns | Output load: 1 TTL load |
| $t_{CO}$ | Chip Select Delay | | 250 | | 300 | ns | and 100 pf |
| $t_{DF}$ | Chip Deselect Delay | | 250 | | 300 | ns | Input transition time: 20ns |
| $t_{OH}$ | Previous Data Valid After Address Change Delay | 20 | | 20 | | ns | Timing reference levels:<br>Input: 1.5V<br>Output: 0.8V and 2.2V |

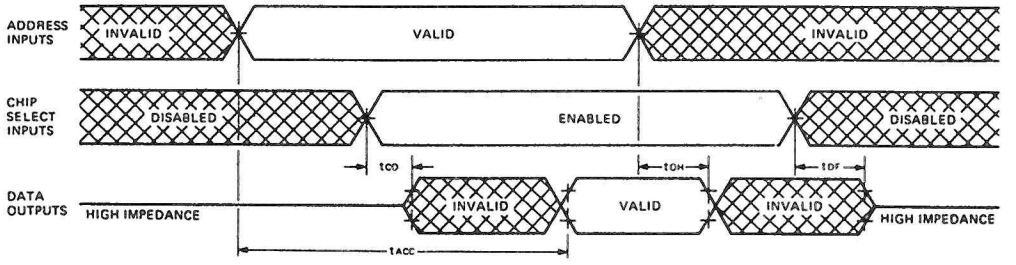
## CAPACITANCE

$t_A$ = 25°C, f = 1.0MHz, See Note 2

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_I$ | Input Capacitance | | 7 | pF | All pins except pin under |
| $C_O$ | Output Capacitance | | 10 | pF | test tied to AC ground |

Note 2: This parameter is periodically sampled and is not 100% tested.

### TIMING DIAGRAM




ROMs

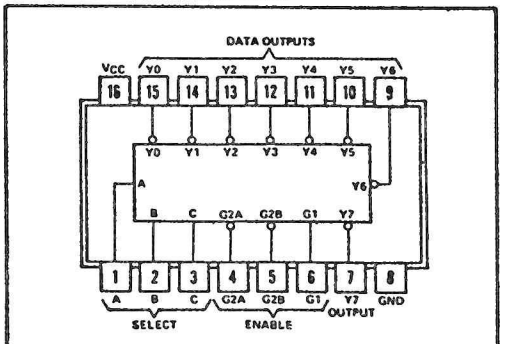
# TYPES SN54LS138, SN54LS139, SN54S138, SN54S139, SN74LS138, SN74LS139, SN74S138, SN74S139 DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7611804, DECEMBER 1972—REVISED OCTOBER 1976

- Designed Specifically for High-Speed:
  Memory Decoders
  Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 'S139 and 'LS139 Contain Two Fully Independent 2-to-4-Line Decoders/ Demultiplexers
- Schottky Clamped for High Performance

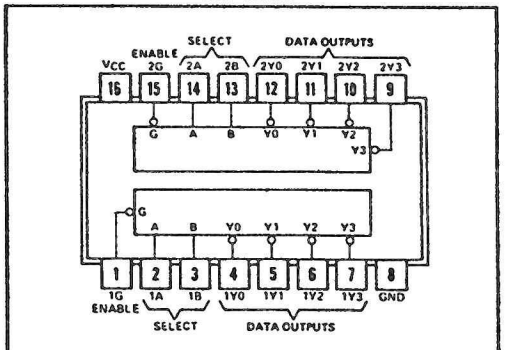
| TYPE | TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC) | TYPICAL POWER DISSIPATION |
|---|---|---|
| 'LS138 | 22 ns | 32 mW |
| 'S138 | 8 ns | 245 mW |
| 'LS139 | 22 ns | 34 mW |
| 'S139 | 7.5 ns | 300 mW |

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)




positive logic: see function table

SN54LS139, SN54S139 . . . J OR W PACKAGE
SN74LS139, SN74S139 . . . J OR N PACKAGE
(TOP VIEW)




positive logic: see function table

## description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 'LS139 and 'S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74LS load ('LS138, 'LS139) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.



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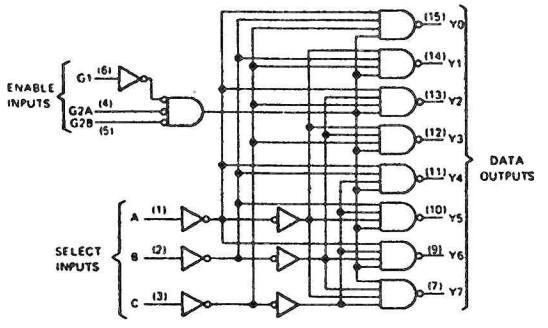
## functional block diagrams and logic

'LS138, 'S138



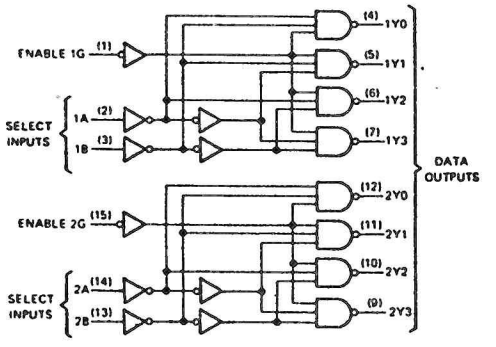

'LS138, 'S138
FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | SELECT | | | | | | | | | | |
| G1 | G2* | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

'LS139, 'S139



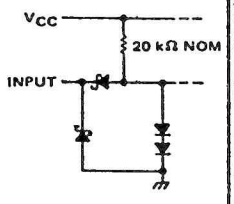

'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| ENABLE | SELECT | | | | | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

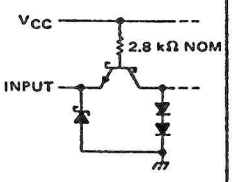
H = high level, L = low level, X = irrelevant

## schematics of inputs and outputs

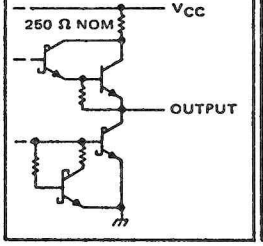
EQUIVALENT OF EACH INPUT OF 'LS138, 'LS139



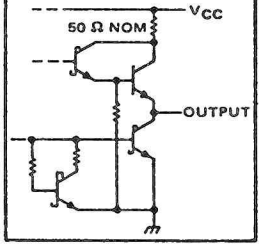

EQUIVALENT OF EACH INPUT OF 'S138, 'S139




TYPICAL OF OUTPUTS OF 'LS138, 'LS139




TYPICAL OF OUTPUTS OF 'S138, 'S139



## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3446 | 0°C to +70°C | Plastic DIP |

# MC3446

## QUAD GENERAL PURPOSE INTERFACE BUS (G.P.I.B.) TRANSCEIVER

The MC3446 is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1975 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with Hewlett Packard Interface Bus. (HP-IB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power – Average Power Supply Current = 12 mA
- Termination Resistors Provided

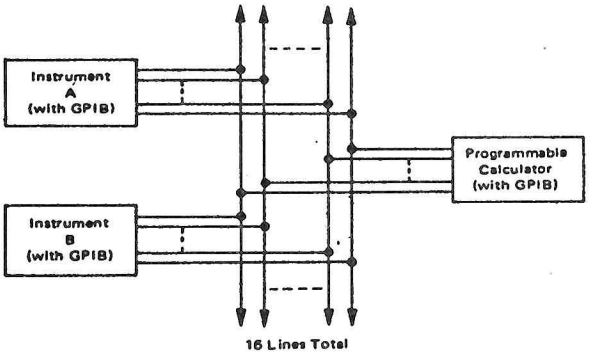
## QUAD INTERFACE BUS TRANSCEIVER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

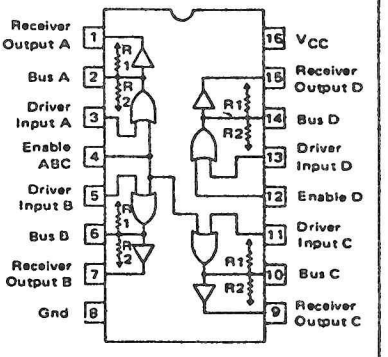
P SUFFIX
PLASTIC PACKAGE
CASE 648

5

### TYPICAL MEASUREMENT SYSTEM APPLICATION




### PIN CONNECTIONS




R1 = 2.4 k
R2 = 5.0 k

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Driver Output Current | $I_{O(D)}$ | 150 | mA |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, 4.75 V ≤ $V_{CC}$ ≤ 5.25 V and 0 ≤ $T_A$ ≤ 70°C, typical values are at $T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DRIVER PORTION** | | | | | |
| Input Voltage – High Logic State | $V_{IH(D)}$ | 2.0 | – | – | V |
| Input Voltage – Low Logic State | $V_{IL(D)}$ | – | – | 0.8 | V |
| Input Current – High Logic State ($V_{IH}$ = 2.4 V) | $I_{IH(D)}$ | – | 5.0 | 20 | µA |
| Input Current – Low Logic State ($V_{IL}$ = 0.4 V, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $I_{IL(D)}$ | – | 0.2 | 0.36 | mA |
| Input Clamp Voltage ($I_{IC}$ = -12 mA) | $V_{IC(D)}$ | – | – | -1.5 | V |
| Output Voltage – High Logic State (1) ($V_{IH(S)}$ = 2.4 V or $V_{IH(D)}$ = 2.0 V) | $V_{OH(D)}$ | 2.5 | 3.3 | 3.7 | V |
| Output Voltage – Low Logic State ($V_{IL(S)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA) | $V_{OL(D)}$ | – | – | 0.4 | |
| Input Breakdown Current ($V_{I(D)}$ = 5.5 V) | $I_{IB(D)}$ | – | – | 1.0 | mA |
| **RECEIVER PORTION** | | | | | |
| Input Hysteresis | – | 400 | 900 | – | mV |
| Input Threshold Voltage – Low to High Output Logic State | $V_{ILH(R)}$ | – | 1.78 | 2.0 | V |
| Input Threshold Voltage – High to Low Output Logic State | $V_{IHL(R)}$ | 0.6 | 0.88 | – | V |
| Output Voltage – High Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OH(R)}$ = -400 µA) | $V_{OH(R)}$ | 2.4 | – | – | V |
| Output Voltage – Low Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OL(R)}$ = 8.0 mA) | $V_{OL(R)}$ | – | – | 0.4 | V |
| Output Short-Circuit Current ($V_{IH(R)}$ = 2.0 V) (Only one output may be shorted at a time) | $I_{OS(R)}$ | 4.0 | – | 14 | mA |
| **BUS LOAD CHARACTERISTICS** | | | | | |
| Bus Voltage ($V_{IH(E)}$ = 2.4 V, $I_{BUS}$ = -12 mA) | $V_{(BUS)}$ | 2.5<br>– | 3.3<br>– | 3.7<br>-1.5 | V |
| Bus Current ($V_{IH(O)}$ = 2.4 V, $V_{BUS}$ ≥ 5.0 V)<br>($V_{IH(D)}$ = 2.4 V, $V_{BUS}$ = 0.4 V)<br>($V_{BUS}$ ≤ 5.5 V) | $I_{(BUS)}$ | 0.7<br>-1.3<br>– | –<br>–<br>– | –<br>-3.2<br>2.5 | mA |
| **TOTAL DEVICE POWER CONSUMPTION** | | | | | |
| Power Supply Current (All Drivers OFF)<br>(All Drivers ON) | $I_{CC}$ | –<br>– | 12<br>32 | 19<br>39 | mA |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DRIVER PORTION** | | | | | |
| Propagation Delay Time from Driver Input to Low Logic State Bus Output | $t_{PHL(D)}$ | – | 34 | 50 | ns |
| Propagation Delay Time from Driver Input to High Logic State Bus Output | $t_{PLH(D)}$ | – | 17 | 40 | ns |
| Propagation Delay Time from Enable Input to Low Logic State Bus Output | $t_{PHL(E)}$ | – | 39 | 50 | ns |
| Propagation Delay Time from Enable Input to High Logic State Bus Output | $t_{PLH(E)}$ | – | 32 | 50 | ns |
| **RECEIVER PORTION** | | | | | |
| Propagation Delay Time from Bus Input to High Logic State Receiver Output | $t_{PLH(R)}$ | – | 37 | 50 | ns |
| Propagation Delay Time from Bus Input to Low Logic State Receiver Output | $t_{PHL(R)}$ | – | 22 | 40 | ns |

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# SY6500

## SY6500 MICROPROCESSORS

### The SY6500 Microprocessor Family Concept ----

The SY6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock osscillators and drivers. All of the microprocessors in the SY6500 group are software compatible within the group and are bus compatible with the M6800 product offering.

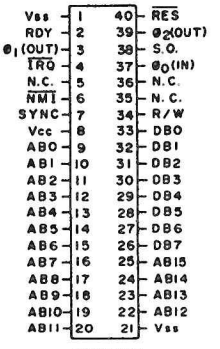
The family includes five microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for the multi processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz and 2 MHz ("A" suffix on product numbers) maximum operating frequencies.

### Features of the SY6500 Family

- Single five volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- Bi-directional Data Bus
- Instruction decoding and control
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1MHz and 2MHz operation
- On-the-chip clock options
  - * External single clock input
  - * RC time base input
  - * Crystal time base input
- 40 and 28 pin package versions
- Pipeline architecture

MICRO PROCESSORS

### SY6502 – 40 Pin Package



SY6502

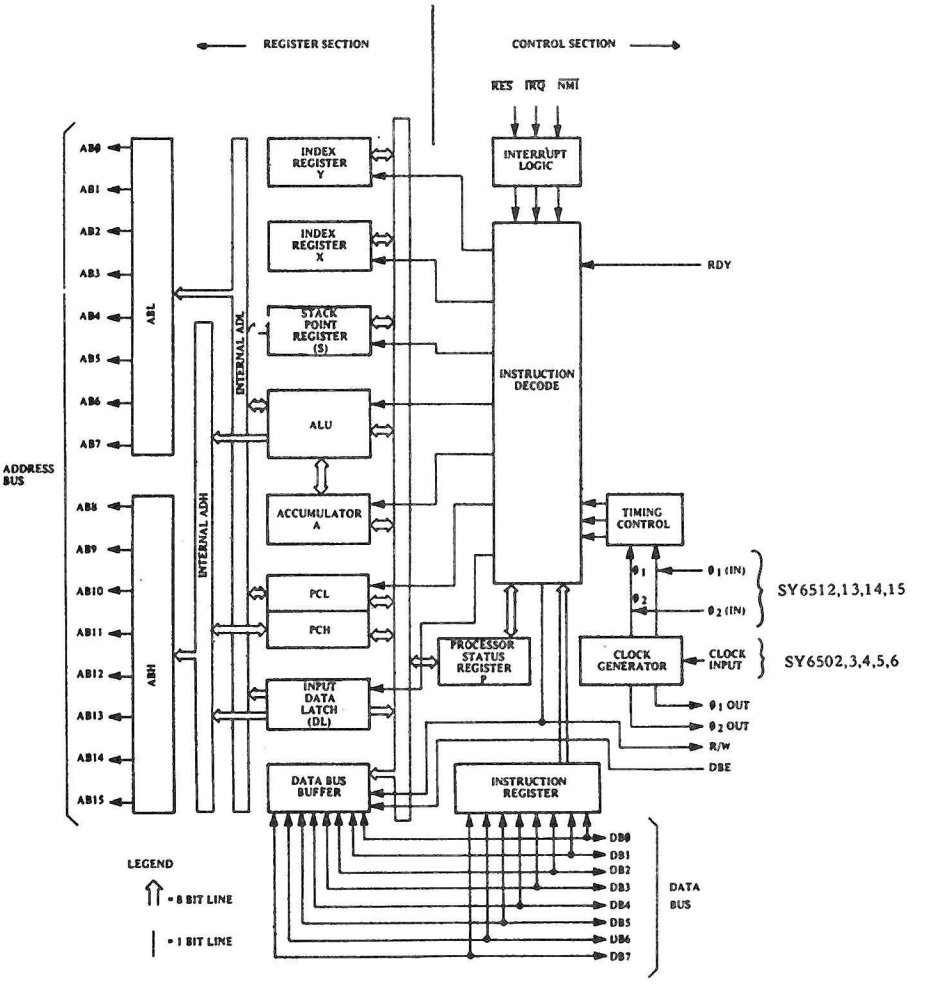
* 65K Addressable Bytes of Memory
* $\overline{IRQ}$ Interrupt * $\overline{NMI}$ Interrupt
* On-the-chip Clock
  - ✓ TTL Level Single Phase Input
  - ✓ RC Time Base Input
  - ✓ Crystal Time Base Input
* SYNC Signal
  (can be used for single instruction execution)
* RDY Signal
  (can be used for single cycle execution)
* Two Phase Output Clock for Timing of Support Chips

**Features of SY6502**

## Comments on the Data Sheet

The data sheet is constructed to review first the basic "Common Characteristics" - those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

## COMMON CHARACTERISTICS




Note: 1. Clock Generator is not included on SY6512,13,14,15
2. Addressing Capability and control options vary with each of the SY6500 Products.

**SY6500 Internal Architecture**

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3050 Coronado Drive, Santa Clara, CA. 95051
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SY6520

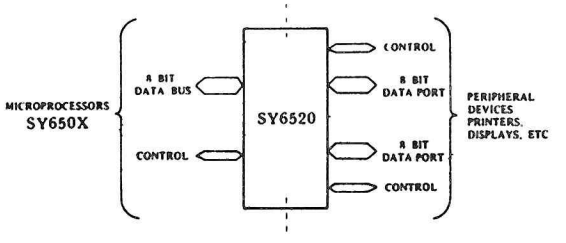
# SY6520 PERIPHERAL ADAPTER

## DESCRIPTION

The SY6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the SY6500 family of microprocessors, the SY6520 allows implementation of very complex systems at a minimum overall cost.

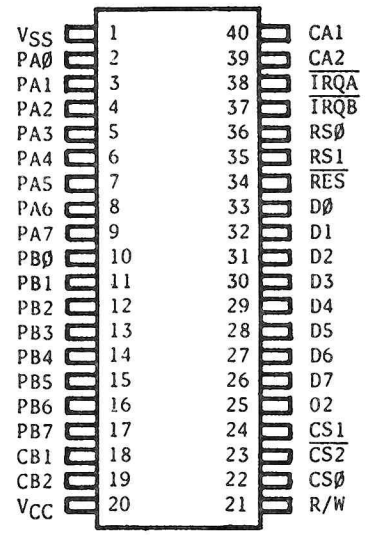
Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

- High performance replacement for Motorola/AMI/MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.




*Basic SY6520 Interface Diagram*

SY6520




MICRO-PROCESSORS

# SUMMARY OF SY6520 OPERATION

See SYNERTEK Microcomputer Hardware Manual for detailed description of SY6520 operation.

## CA1/CBI CONTROL

| CRA (CRB) Bit 1 | CRA (CRB) Bit 0 | Active Transition of Input Signal* | IRQA (IRQB) Interrupt Outputs |
|---|---|---|---|
| 0 | 0 | negative | Disable--remain high |
| 0 | 1 | negative | Enable--goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1) |
| 1 | 0 | positive | Disable--remain high |
| 1 | 1 | positive | Enable--as explained above |

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

## CA2/CB2 INPUT MODES

| CRA (CRB) Bit 5 | CRA (CRB) Bit 4 | CRA (CRB) Bit 3 | Active Transition of Input Signal* | IRQA (IRQB) Interrupt Output |
|---|---|---|---|---|
| 0 | 0 | 0 | negative | Disable--remains high |
| 0 | 0 | 1 | negative | Enable--goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2) |
| 0 | 1 | 0 | positive | Disable--remains high |
| 0 | 1 | 1 | positive | Enable--as explained above |

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

MICRO-PROCESSORS

## CA2 OUTPUT MODES

| CRA Bit 5 | CRA Bit 4 | CRA Bit 3 | Mode | Description |
|---|---|---|---|---|
| 1 | 0 | 0 | "Handshake" on Read | CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor. |
| 1 | 0 | 1 | Pulse Output | CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken. |
| 1 | 1 | 0 | Manual Output | CA2 set low |
| 1 | 1 | 1 | Manual Output | CA2 set high |

## CB2 OUTPUT MODES

| CRB Bit 5 | CRB Bit 4 | CRB Bit 3 | Mode | Description |
|---|---|---|---|---|
| 1 | 0 | 0 | "Handshake" on Write | CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device. |
| 1 | 0 | 1 | Pulse Output | CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available. |
| 1 | 1 | 0 | Manual Output | CB2 set low |
| 1 | 1 | 1 | Manual Output | CB2 set high |

Synertek®

3050 Coronado Drive, Santa Clara, CA. 95051
(408) 984-8900 TWX 910-338-0135

# SY6522

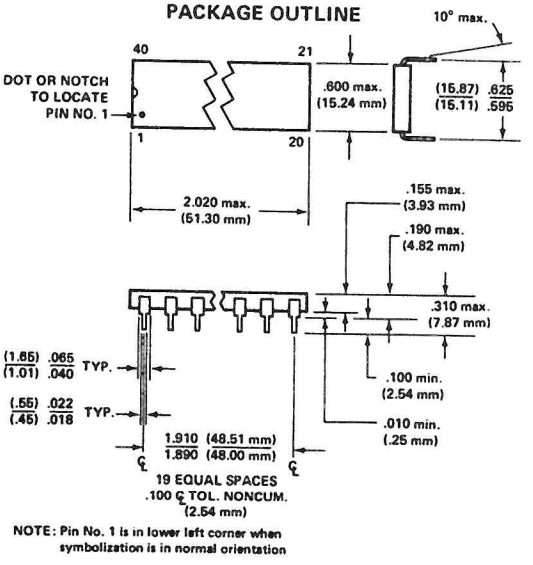
## SY6522 (VERSATILE INTERFACE ADAPTER)

The SY6522 Versatile Interface Adapter (VIA) provides all of the capability of the SY6520. In addition, this device contains a pair of very powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

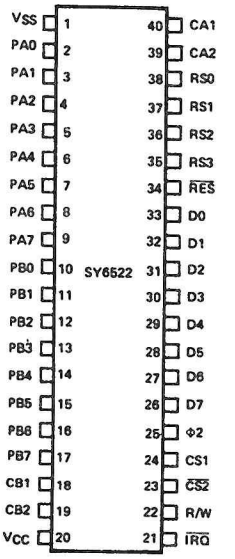
Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. Also, several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves and for counting externally generated pulses. To facilitate control of the many powerful features of this chip, the internal registers have been organized into an interrupt flag register, an interrupt enable register and a pair of function control registers.

- Very powerful expansion of basic SY6520 capability.
- N channel, depletion load technology, single +5V Supply.
- Completely static and TTL compatible.
- CMOS compatible peripheral control lines.
- Expanded "handshake" capability allows very positive control of data transfers between processor and peripheral devices.

PACKAGE OUTLINE




NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation



## MAXIMUM RATINGS

| | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | Vcc | -0.3 to +7.0 | Vdc |
| Input Voltage | Vin | -0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -55 to +150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

**Electrical Characteristics ($V_{CC}$ = 5.0V ±5%, $V_{SS}$ = 0, $T_A$ = 0°C to 70°C unless otherwise noted)**

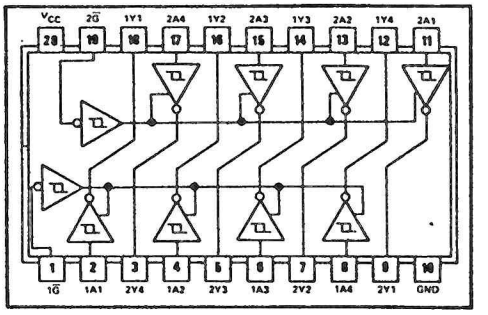
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input high voltage (normal operation) | $V_{IH}$ | +2.4 | – | Vcc | Vdc |
| Input Low Voltage (normal operation) | $V_{IL}$ | -0.3 | – | +0.4 | Vdc |
| Input Leakage current - $V_{IN}$ = 0 to 5 Vdc<br>R/W, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, Φ2 | $I_{IN}$ | – | ±1.0 | ±2.5 | μAdc |
| Off-state input current - $V_{IN}$ = .4 to 2.4 V<br>Vcc = Max, D0 to D7 | $I_{TSI}$ | – | ±2.0 | ±10 | μAdc |
| Input high current - $V_{IH}$ = 2.4 V<br>PA0 - PA7, CA2, PB0 - PB7, CB1, CB2 | $I_{IH}$ | -100 | -250 | – | μAdc |
| Input low current - $V_{IL}$ = 0.4 Vdc<br>PA0 - PA7, CA2, PB0 - PB7, CB1, CB2 | $I_{IL}$ | – | -1.0 | -1.6 | mAdc |
| Output high voltage<br>Vcc = min, $I_{load}$ = -100 μAdc<br>PA0 - PA7, CA2, PB0 -PB7, CB1, CB2 | $V_{OH}$ | 2.4 | – | – | Vdc |
| Output low voltage<br>Vcc = min, $I_{load}$ = 1.6 mAdc | $V_{OL}$ | – | – | +0.4 | Vdc |
| Output high current (sourcing)<br>$V_{OH}$ = 2.4 V<br>$V_{OH}$ = 1.5 V, PB0 - PB7, CB1, CB2 | $I_{OH}$ | <br>-100<br>-3.0 | <br>-1000<br>-5.0 | <br>–<br>– | <br>μAdc<br>mAdc |
| Output low current (sinking)<br>$V_{OL}$ = 0.4 Vdc | $I_{OL}$ | 1.6 | – | – | mAdc |
| Output leakage current (off state)<br>$\overline{IRQ}$ | $I_{off}$ | – | 1.0 | 10 | μAdc |
| Input capacitance - $T_A$ = 25°C, f = 1 Mhz<br>R/W, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$<br>D0 - D7, PA0 - PA7, CA1, CA2, PB0 - PB7, CB1, CB2<br>Φ2 input | $C_{in}$ | <br>–<br>– | <br>–<br>– | <br>7.0<br>10 | <br>pF<br>pF |
| | | – | – | 20 | pF |
| Output capacitance - $T_A$ = 25°C, f = 1 Mhz | $C_{out}$ | – | – | 10 | pF |
| Power dissipation | $P_d$ | – | – | 1000 | MW |

# TYPES SN54LS240,SN54LS241,SN54LS244,SN54S240,SN54S241, SN74LS240,SN74LS241,SN74LS244,SN74S240,SN74S241 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

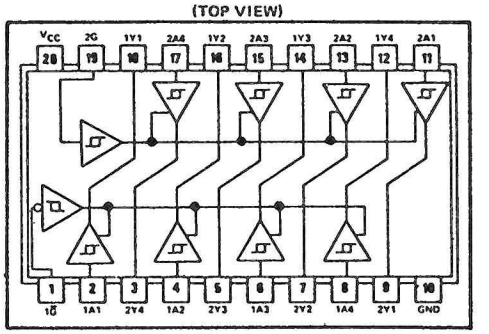
| | Typical $I_{OL}$ (Sink Current) | Typical $I_{OH}$ (Source Current) | Typical Propagation Delay Times | | Typical Enable/ Disable Times | Typical Power Dissipation (Enabled) | |
|---|---|---|---|---|---|---|---|
| | | | Inverting | Noninverting | | Inverting | Noninverting |
| SN54LS' | 12 mA | −12 mA | 10.5 ns | 12 ns | 18 ns | 130 mW | 135 mW |
| SN74LS' | 24 mA | −15 mA | 10.5 ns | 12 ns | 18 ns | 130 mW | 135 mW |
| SN54S' | 48 mA | −12 mA | 4.5 ns | 6 ns | 9 ns | 450 mW | 538 mW |
| SN74S' | 64 mA | −15 mA | 4.5 ns | 6 ns | 9 ns | 450 mW | 538 mW |

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

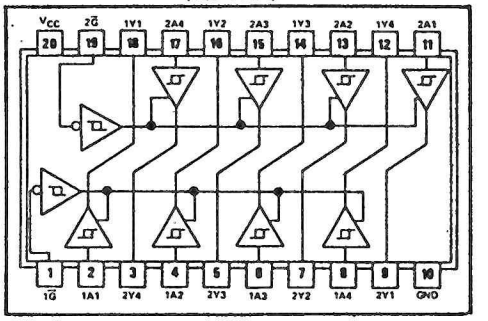
SN54LS240, SN54S240 . . . J
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)




SN54LS241, SN54S241 . . . J
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)




SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)

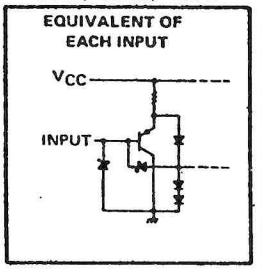



## description

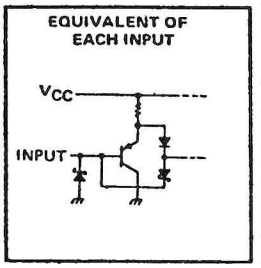
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

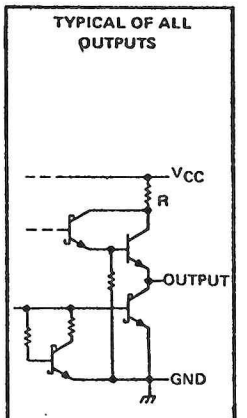
## schematics of inputs and outputs

'LS240, 'LS241, 'LS244




'S240 'S241




'LS240, 'LS241, 'LS244:
R = 50 Ω NOM
'S240, 'S241:
R = 25 Ω NOM

6

# TYPES SN54100, SN74100
# 8-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7211830, DECEMBER 1972

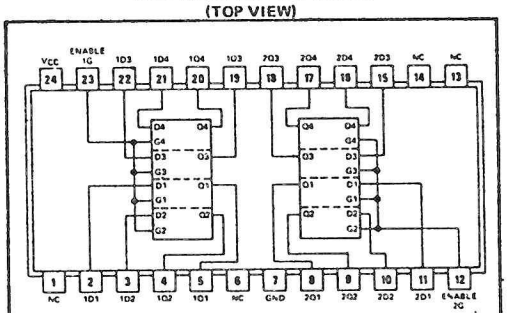
## logic

FUNCTION TABLE
(Each Latch)

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| D | G | Q | $\bar{Q}$ |
| L | H | L | H |
| H | H | H | L |
| X | L | $Q_0$ | $\bar{Q}_0$ |

H = high level, X = irrelevant
$Q_0$ = the level of Q before the high-to-low transition of G

SN54100 . . . J OR W PACKAGE
SN54100 . . . J OR N PACKAGE
(TOP VIEW)




positive logic: see function table

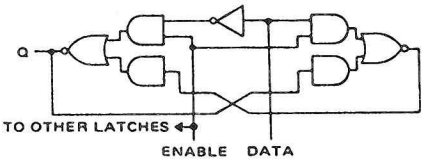
NC—No internal connection

## description

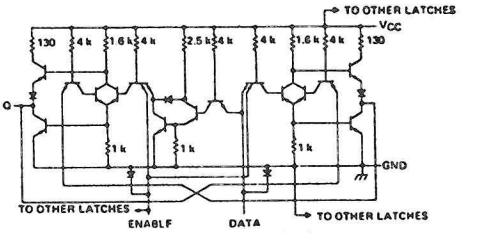
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was setup at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 40 milliwatts per latch. The SN54100 is characterized for operation over the full military temperature range of −55° to 125°C; the SN74100 is characterized for operation from 0°C to 70°C.

## functional block diagram (each latch)




## schematic (each latch)




Resistor values shown are nominal and in ohms.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Intermitter voltage (see Note 2) | 5.5 V |
| Operating free-air temperature range: SN54100 | −55°C to 125°C |
| SN74100 | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. For this circuit, this rating applies between the enable and D inputs of any latch.

# TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74L157, SN74LS157, SN74LS158, SN74S157, SN74S158
# QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7711847, MARCH 1974—REVISED AUGUST 1977

## features

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

| TYPES | TYPICAL AVERAGE PROPAGATION TIME | TYPICAL POWER DISSIPATION |
|---|---|---|
| '157 | 9 ns | 150 mW |
| 'L157 | 18 ns | 75 mW |
| 'LS157 | 9 ns | 49 mW |
| 'S157 | 5 ns | 250 mW |
| 'LS158 | 7 ns | 24 mW |
| 'S158 | 4 ns | 195 mW |

## applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

## description

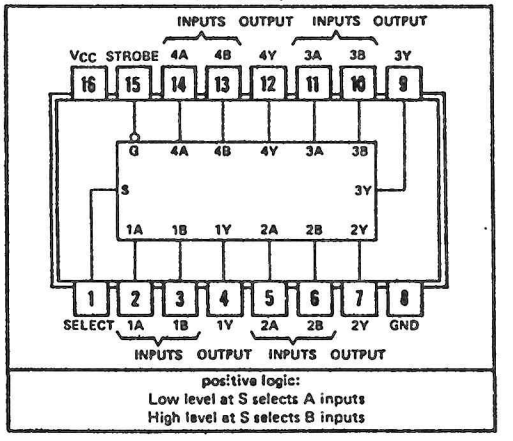
These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

| INPUTS | | | | OUTPUT Y | |
|---|---|---|---|---|---|
| STROBE | SELECT | A | B | '157, 'L157, 'LS157, 'S157 | 'LS158 'S158 |
| H | X | X | X | L | H |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

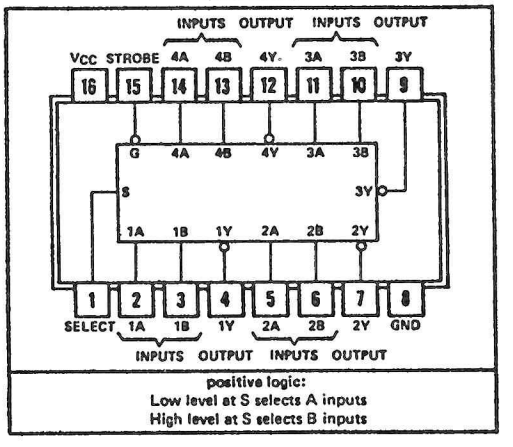
H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157 . . . J OR W PACKAGE
SN54L157 . . . J PACKAGE
SN74157, SN74L157, SN74LS157, SN74S157 . . . J OR N PACKAGE
(TOP VIEW)




positive logic:
Low level at S selects A inputs
High level at S selects B inputs

SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74LS158, SN74S158 . . . J OR N PACKAGE
(TOP VIEW)




positive logic:
Low level at S selects A inputs
High level at S selects B inputs

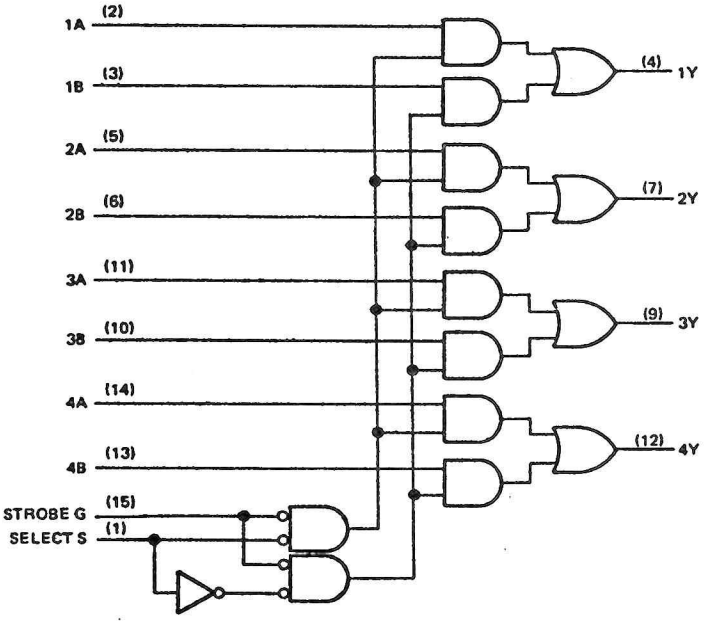
## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '157, 'L157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

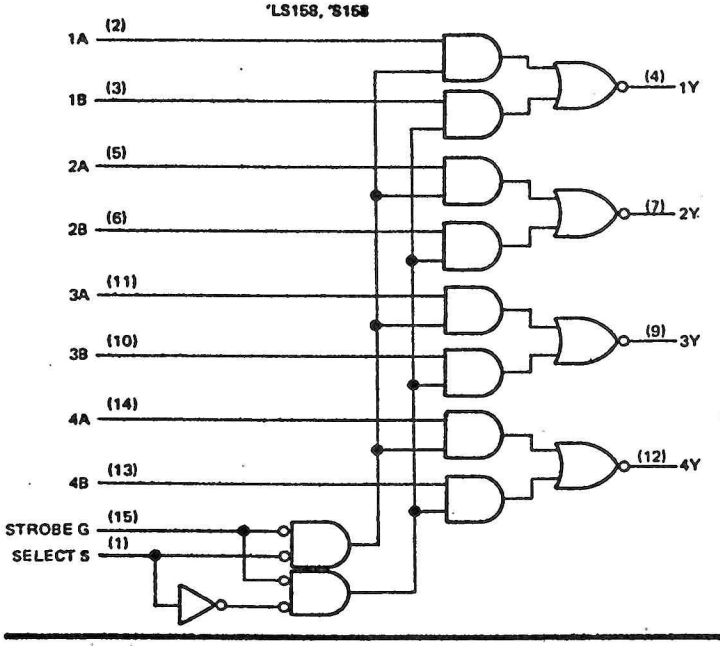
NOTE 1: Voltage values are with respect to network ground terminal.

## functional block diagrams

'LS157, 'S157

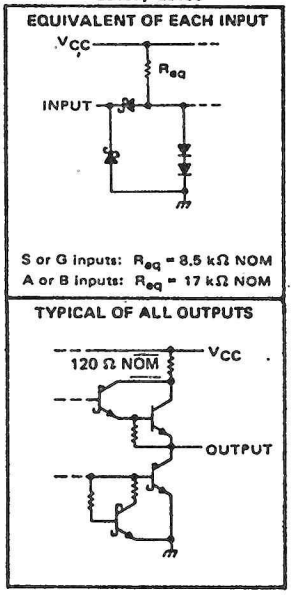



'LS158, 'S158

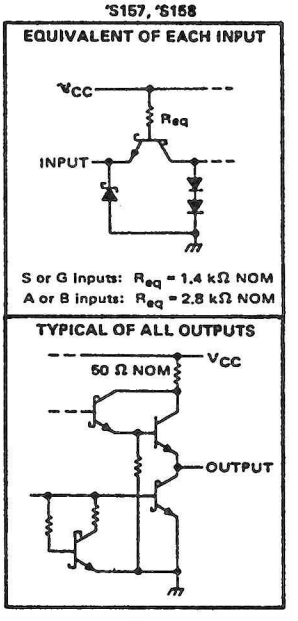



## schematics of inputs and outputs

'LS157, 'LS158

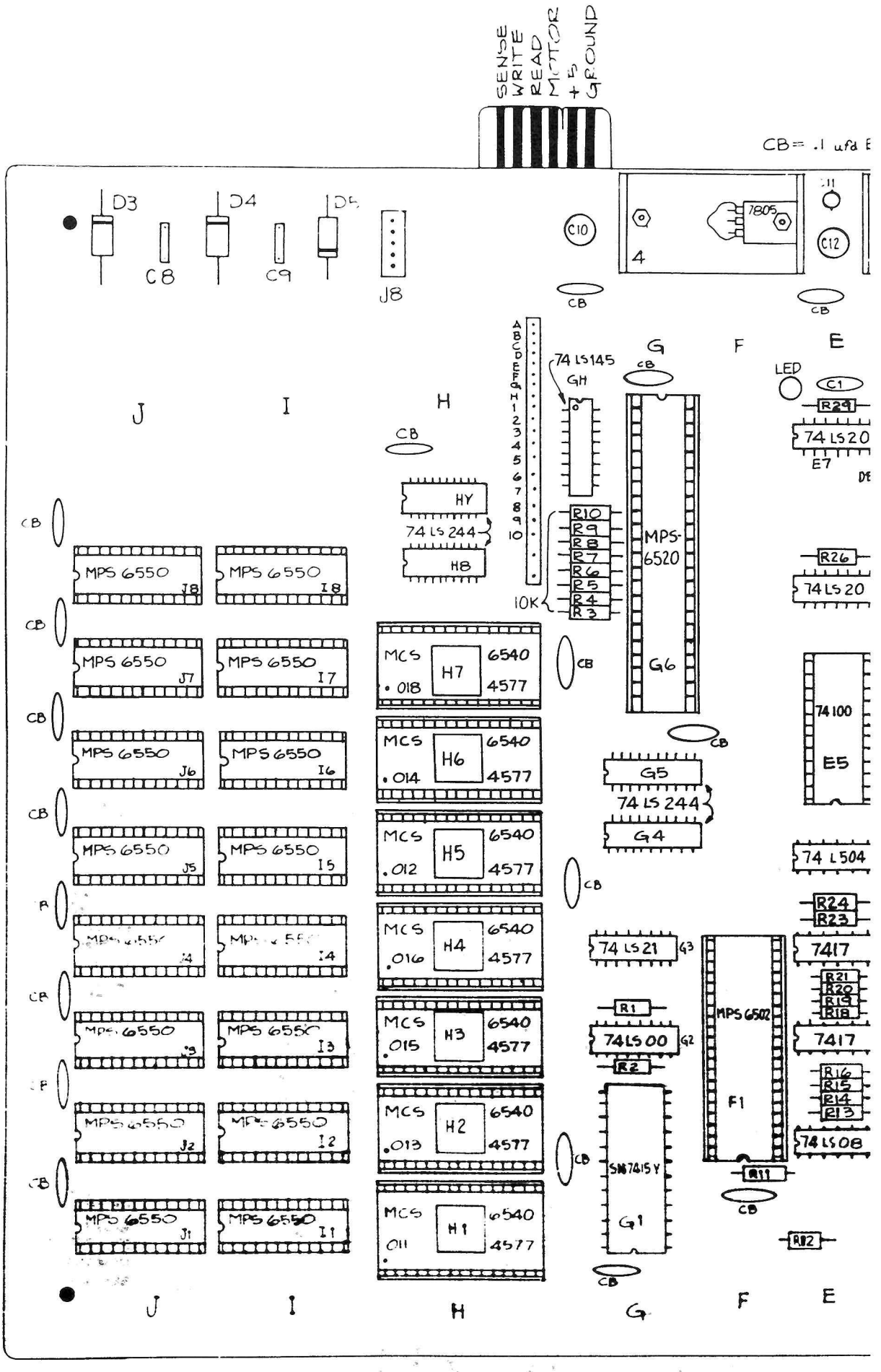



'S157, 'S158



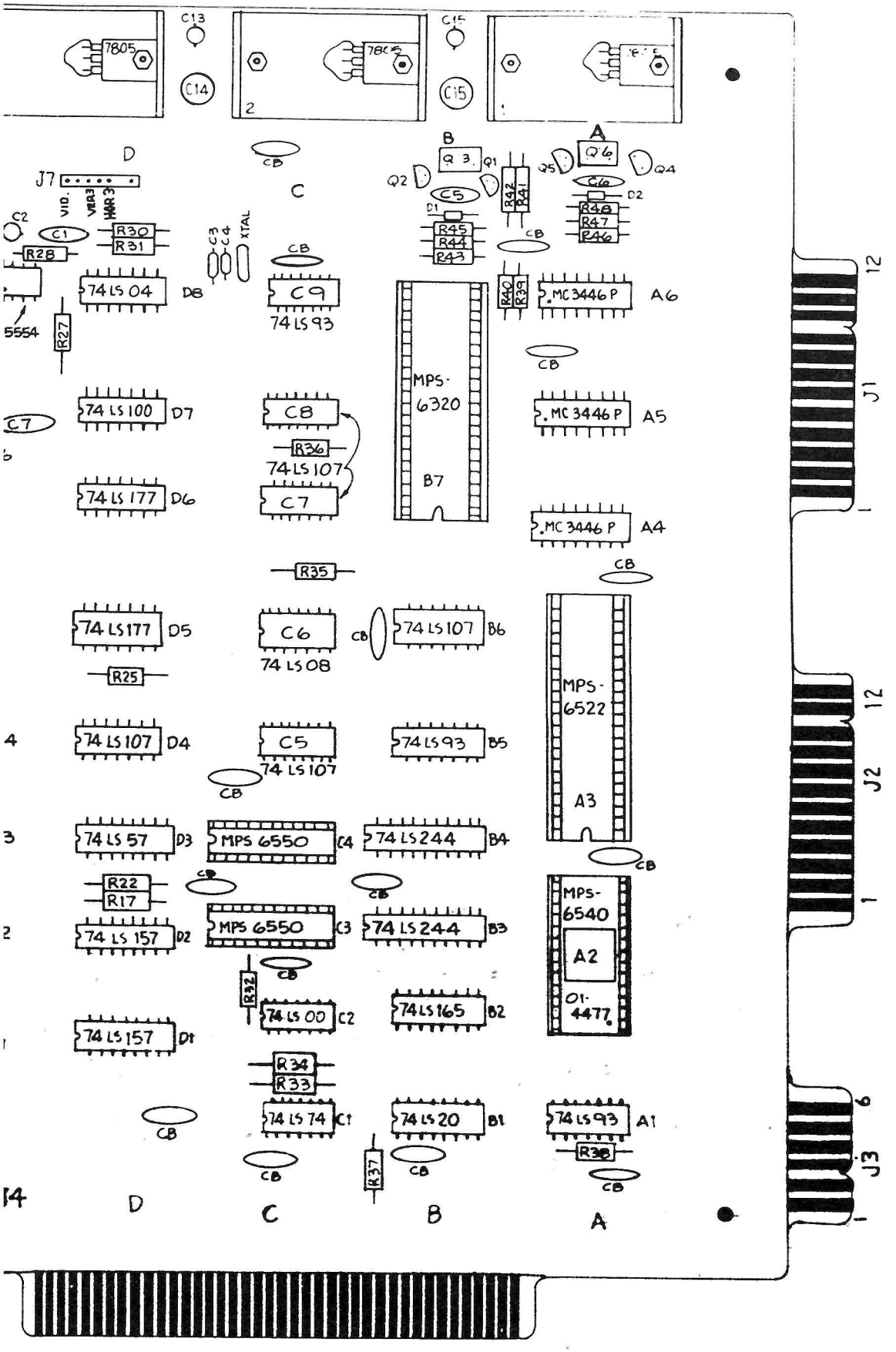

7

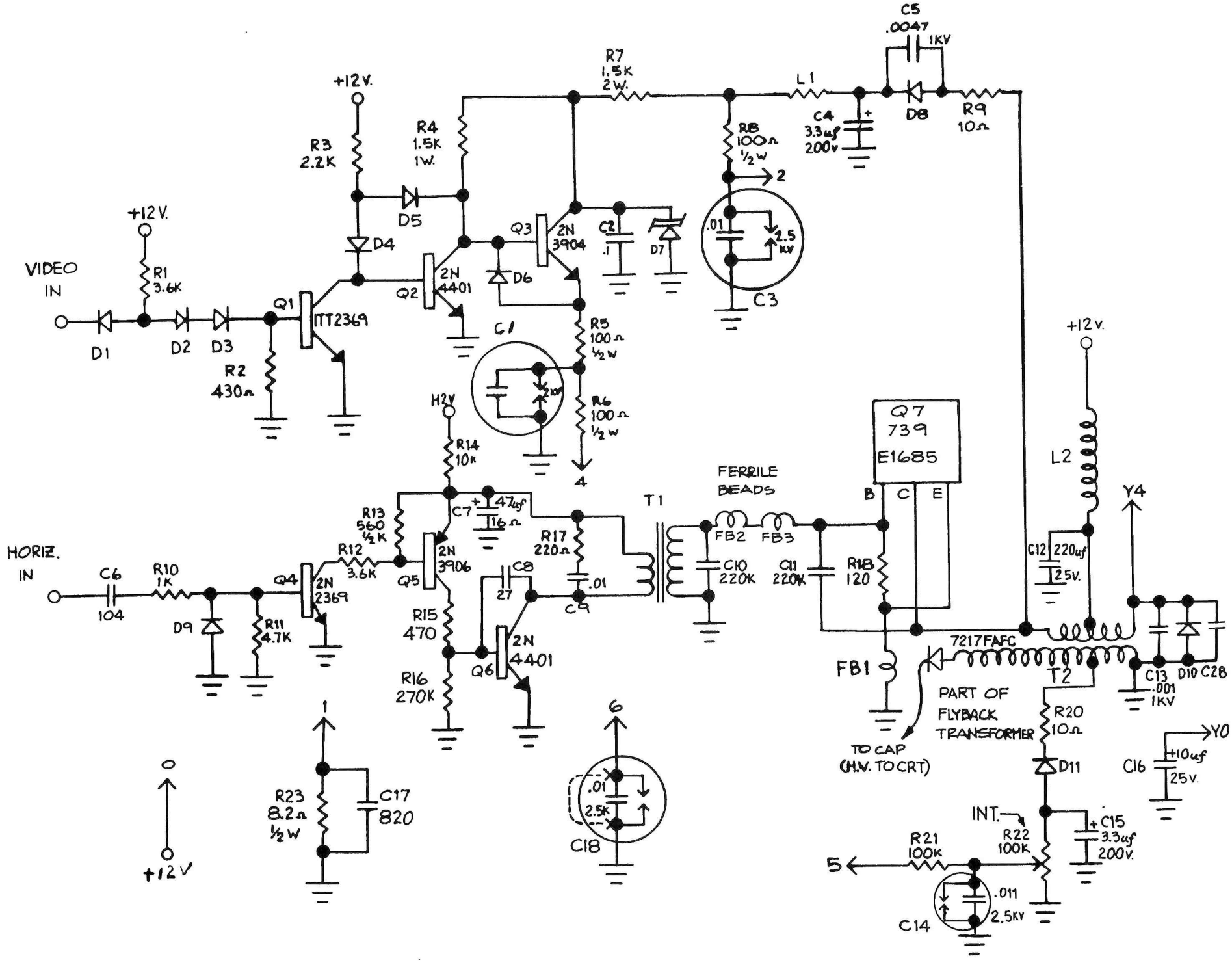
076

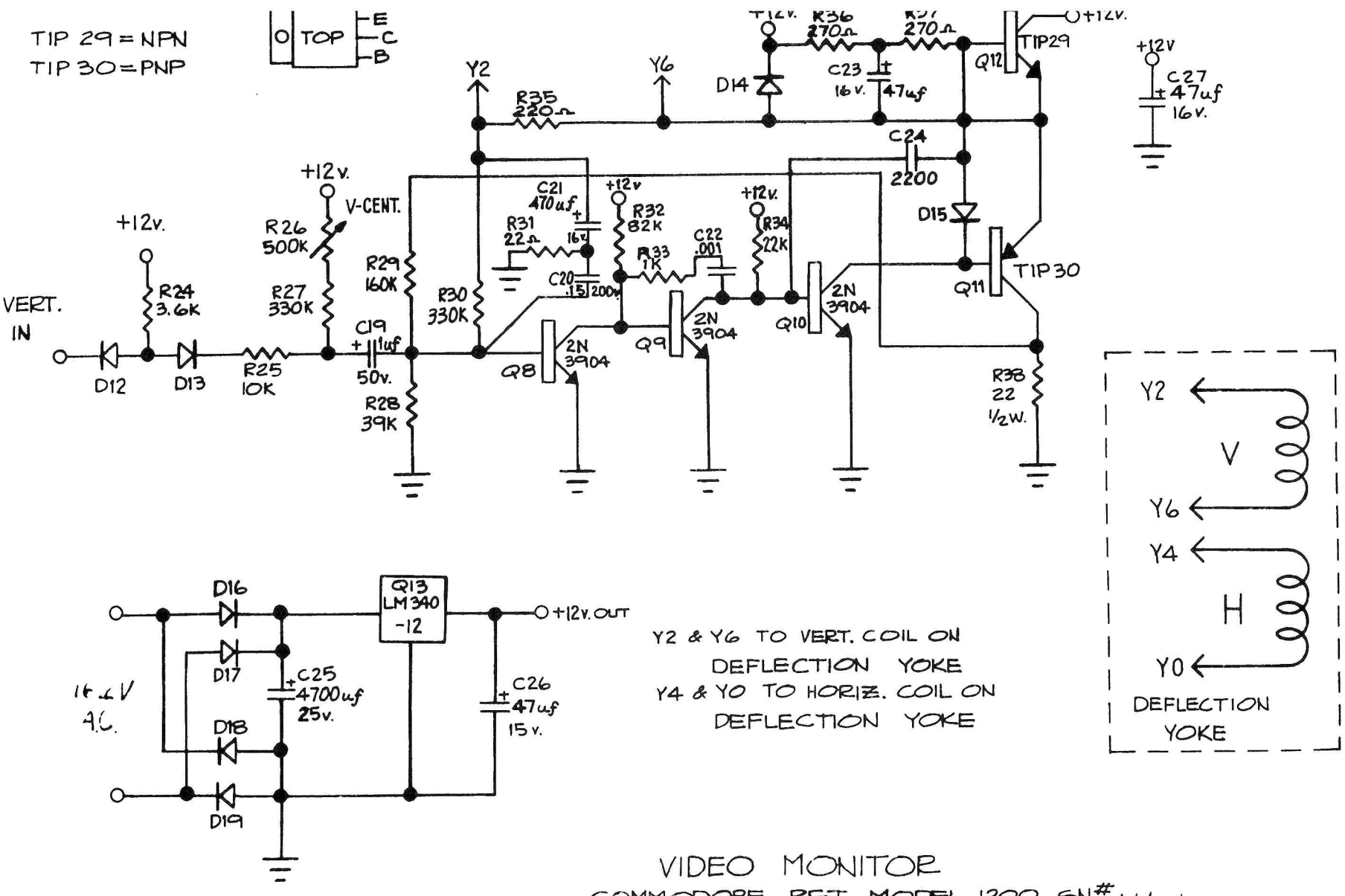



PET CPU BOARD

ASS CAPACITORS




+12V.
R3
2.2K
R4
1.5K
1W.
R7
1.5K
2W.
L1
C5
.0047
1KV
C4
3.3uf
200v
D8
R9
10Ω
R8
100Ω
½W
2
.01
2.5
KV
C3
D5
D4
Q3
2N
3904
C2
.1
D7
D6
+12V.
VIDEO
IN
R1
3.6K
Q1
TT2369
Q2
2N
4401
C1
D1
D2
D3
R2
430Ω
R5
100Ω
½W
R6
100Ω
½W
H2V
R14
10K
4
FERRILE
BEADS
T1
Q7
739
E1685
B
C
E
L2
+12V.
Y4
R13
560
½K
C7
47uf
16v
R12
3.6K
Q5
2N
3906
R17
220Ω
.01
C9
C8
27
FB2
FB3
C10
220K
C11
220K
R18
120
C12
220uf
25V.
HORIZ.
IN
C6
104
R10
1K
Q4
2N
2369
D9
R11
4.7K
R15
470
R16
270K
Q6
2N
4401
7217FAFC
T2
FB1
PART OF
FLYBACK
TRANSFORMER
TO CAP
(H.V. TO CRT)
C13
.001
1KV
D10
C28
R20
10Ω
D11
Y0
C16
+10uf
25V.
INT.
R21
100K
R22
100K
+C15
3.3uf
200V.
5
.011
2.5KV
C14
1
R23
8.2Ω
½W
C17
820
6
.01
2.5K
C18
0
+12V




# VIDEO MONITOR

COMMODORE PET MODEL 1200 SN# 11151

PET-SHACK SOFTWARE HOUSE